

MALLA REDDY ENGINEERING COLLEGE

(Autonomous)

LECTURE NOTES

ON

ELECTRONIC CIRCUITS AND PULSE CIRCUITS

(80410)

B.Tech-ECE-IV semester

Mrs.P.Sowjanya

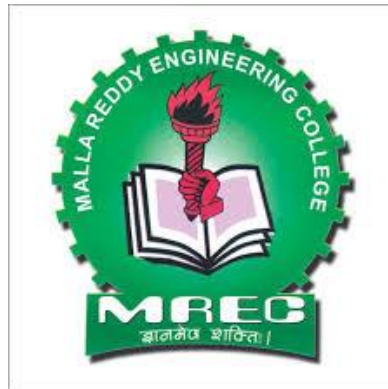
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ELECTRONICS AND COMMUNICATION ENGINEERING

MALLA REDDY ENGINEERING COLLEGE (Autonomous)

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| 2018-19 Onwards (MR-18) | MALLA REDDY ENGINEERING COLLEGE (Autonomous) | B.Tech. IV Semester | | |
| Code: 80410 | ELECTRONIC CIRCUITS & PULSE CIRCUITS | L | T | P |
| Credits: 4 | | 3 | 1 | - |

Pre-Requisites: Basic Electrical and Electronic Engineering, Analog Electronics.

Course Objectives: This course provides the knowledge of Transistor Amplifier particularly Multistage Amplifiers and Power Amplifiers. It provides knowledge of responses of sinusoidal and non-sinusoidal signals to high pass and low pass RC circuits. It also introduces Diode and Transistor Clippers and Clampers along with reference voltages. It provides knowledge of Diode and Transistor switching times and Design and Applications of Multivibrators and Schmitt trigger.

MODULE I: Multistage Amplifiers

[14 Periods]

Multistage Amplifiers: Different Coupling Schemes used in Amplifiers, General Analysis of Cascaded RC Coupled BJT Amplifiers Choice of Transistor configuration in a Cascade Amplifier, RC Coupled Amplifier, Transformer Coupled Amplifier, Direct Coupled (DC) Amplifiers, and Darlington Pair. Frequency Response: General Frequency Considerations, High Frequency Hybrid π Model for Common Emitter Transistor Model, Emitter Follower at Higher Frequencies, Design of Single -stage RC Coupled Amplifier using BJT.

MODULE II: Large Signal Amplifiers

[12 Periods]

Introduction, Classification Based on Biasing Condition, Class A Large Signal Amplifiers, Second Harmonic Distortion, Higher - Order Harmonic Generation, Transformer Coupled Class an Audio Power Amplifier, Maximum Value of Efficiency of Class A Amplifiers, Class B Amplifier, Efficiency of Class B Amplifier, Push-Pull Amplifier (Class - B), Distortion in Power Amplifiers, Complementary Symmetry (Class B) Push - Pull Amplifier, Thermal Stability, Heat Sink.

MODULE III: Linear Wave Shaping

[12 Periods]

A. High pass & Low pass RC circuits, their response for Sinusoidal, Step, Pulse, Square and Ramp inputs,
B. High pass RC circuit as differentiator and low pass RC circuit as integrator, Attenuators, Compensation, High pass and low pass RL circuits.

MODULE IV: Non - Linear Wave Shaping

[12 Periods]

Non - Linear Wave Shaping: Diode clippers, transistor clippers, clipping at two independent levels, emitter coupled clipper, comparators, applications of voltage comparators, clamping operation, clamping circuits using diode with different inputs, clamping circuit theorem, practical clamping circuits.

Steady State Switching Characteristics of Diodes & Transistors: Diode as a switch, diode switching times, design of transistor as a switch, transistor - switching times.

MODULE V: Multivibrators

[14 Periods]

A: BISTABLE Multivibrators: The stable state of a Bistable Multivibrator, design and analysis of fixed bias and self-biased Bistable Multivibrator, triggering of Bistable Multivibrator, emitter coupled Bistable Multivibrator, and Design and analysis of Schmitt trigger circuit using transistors.

B: MONOSTABLE and ASTABLE Multivibrators: Monostable Multivibrator, design and analysis of collector coupled Monostable Multivibrator and Monostable multi as voltage to - time converter, Astable Multivibrator, collector coupled Astable Multivibrator and Astable multi as voltage – to - frequency converter.

Text Books:

1. S. Salivahanan, N Suresh Kumar, “Electronic Circuit Analysis”, Tata McGraw Hill Education Private Limited, New Delhi, 2ndEdition, 2012.
2. Jacob Milliman, Christos C. Halkias, Chetan D. Parikh “Integrated Electronics - Analog and Digital Circuits and Systems”, Tata McGraw Hill Education Private Limited, New Delhi, 2ndEdition, 2011

Reference Books:

1. G. K. Mithal, “Electronic Devices and Circuits”, Khanna Publishers, New Delhi, 2nd Edition, 1998.
2. David A. Bell “Solid state pulse circuits”, Prentice Hall of India, New Delhi, India. 4th Edition, 2002.

E-Resources:

1. <http://sureshq.blogspot.in/2015/12/pulse-and-digital-circuits-unit-2-and-3.html>
2. <http://wps.pearsoned.com/wps/media/objects/10581/10835513/Chapter4.pdf>
3. <http://www.radio-electronics.com/info/circuits/>
4. <http://electronicsforu.com/>
5. http://www.serialsjournals.com/journal-detail.php?journals_id=315

MODULE I: MULTISTAGE AMPLIFIERS

In practical applications, the output of a single stage amplifier is usually insufficient, though it is a voltage or power amplifier. Hence they are replaced by **Multi-stage transistor amplifiers**.

In Multi-stage amplifiers, the output of first stage is coupled to the input of next stage using a coupling device. These coupling devices can usually be a capacitor or a transformer. This process of joining two amplifier stages using a coupling device can be called as **Cascading**.

The following figure shows a two-stage amplifier connected in cascade.



The overall gain is the product of voltage gain of individual stages.

$$A_V = A_{V1} \times A_{V2} = V_2 V_1 \times V_0 V_2 = V_0 V_1 A_V = A_{V1} \times A_{V2} = V_2 V_1 \times V_0 V_2 = V_0 V_1$$

Where A_V = Overall gain, A_{V1} = Voltage gain of 1st stage, and A_{V2} = Voltage gain of 2nd stage.

If there are **n** number of stages, the product of voltage gains of those **n** stages will be the overall gain of that multistage amplifier circuit.

Purpose of coupling device

The basic purposes of a coupling device are

- To transfer the AC from the output of one stage to the input of next stage.
- To block the DC to pass from the output of one stage to the input of next stage, which means to isolate the DC conditions.

Types of Coupling

Joining one amplifier stage with the other in cascade, using coupling devices form a **Multi-stage amplifier circuit**. There are **four** basic methods of coupling, using these coupling devices such as resistors, capacitors, transformers etc. Let us have an idea about them.

Resistance-Capacitance Coupling

This is the mostly used method of coupling, formed using simple **resistor-capacitor** combination. The capacitor which allows AC and blocks DC is the main coupling element used here.

The coupling capacitor passes the AC from the output of one stage to the input of its next stage. While blocking the DC components from DC bias voltages to effect the next stage. Let us get into the details of this method of coupling in the coming chapters.

Impedance Coupling

The coupling network that uses **inductance** and **capacitance** as coupling elements can be called as Impedance coupling network.

In this impedance coupling method, the impedance of coupling coil depends on its inductance and signal frequency which is **$j\omega L$** . This method is not so popular and is seldom employed.

Transformer Coupling

The coupling method that uses a **transformer as the coupling** device can be called as Transformer coupling. There is no capacitor used in this method of coupling because the transformer itself conveys the AC component directly to the base of second stage.

The secondary winding of the transformer provides a base return path and hence there is no need of base resistance. This coupling is popular for its efficiency and its impedance matching and hence it is mostly used.

Direct Coupling

If the previous amplifier stage is connected to the next amplifier stage directly, it is called as **direct coupling**. The individual amplifier stage bias conditions are so designed that the stages can be directly connected without DC isolation.

The direct coupling method is mostly used when the load is connected in series, with the output terminal of the active circuit element. For example, head-phones, loud speakers etc.

Role of Capacitors in Amplifiers

Other than the coupling purpose, there are other purposes for which few capacitors are especially employed in amplifiers. To understand this, let us know about the role of capacitors in Amplifiers.

The Input Capacitor C_{in}

The input capacitor C_{in} present at the initial stage of the amplifier, couples AC signal to the base of the transistor. This capacitor C_{in} if not present, the signal source will be in parallel to resistor R_2 and the bias voltage of the transistor base will be changed.

Hence C_{in} allows, the AC signal from source to flow into input circuit, without affecting the bias conditions.

The Emitter By-pass Capacitor C_e

The emitter by-pass capacitor C_e is connected in parallel to the emitter resistor. It offers a low reactance path to the amplified AC signal.

In the absence of this capacitor, the voltage developed across R_E will feedback to the input side thereby reducing the output voltage. Thus in the presence of C_e the amplified AC will pass through this.

Coupling Capacitor C_C

The capacitor C_C is the coupling capacitor that connects two stages and prevents DC interference between the stages and controls the operating point from shifting. This is also called as **blocking capacitor** because it does not allow the DC voltage to pass through it.

In the absence of this capacitor, R_C will come in parallel with the resistance R_1 of the biasing network of the next stage and thereby changing the biasing conditions of the next stage.

Amplifier Consideration

For an amplifier circuit, the overall gain of the amplifier is an important consideration. To achieve maximum voltage gain, let us find the most suitable transistor configuration for cascading.

CC Amplifier

- Its voltage gain is less than unity.
- It is not suitable for intermediate stages.

CB Amplifier

- Its voltage gain is less than unity.
- Hence not suitable for cascading.

CE Amplifier

- Its voltage gain is greater than unity.
- Voltage gain is further increased by cascading.

The characteristics of CE amplifier are such that, this configuration is very suitable for cascading in amplifier circuits. Hence most of the amplifier circuits use CE configuration.

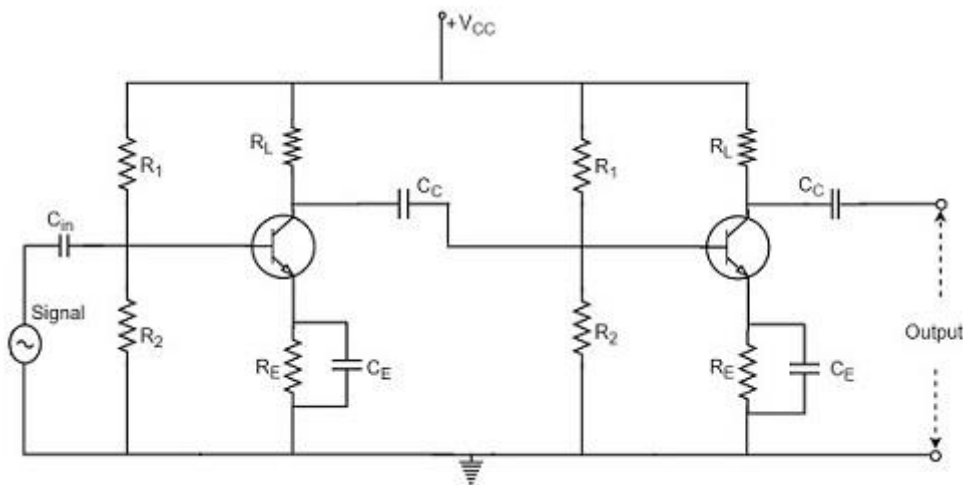
In the subsequent chapters of this tutorial, we will explain the types of coupling amplifiers.

The resistance-capacitance coupling is, in short termed as RC coupling. This is the mostly used coupling technique in amplifiers.

Construction of a Two-stage RC Coupled Amplifier

The constructional details of a two-stage RC coupled transistor amplifier circuit are as follows. The two stage amplifier circuit has two transistors, connected in CE configuration and a common power supply V_{CC} is used. The potential divider network R_1 and R_2 and the resistor R_e form the biasing and stabilization network. The emitter by-pass capacitor C_e offers a low reactance path to the signal.

The resistor R_L is used as a load impedance. The input capacitor C_{in} present at the initial stage of the amplifier couples AC signal to the base of the transistor. The capacitor C_C is the coupling capacitor that connects two stages and prevents DC interference between the stages and controls the shift of operating point. The figure below shows the circuit diagram of RC coupled amplifier.



Operation of RC Coupled Amplifier

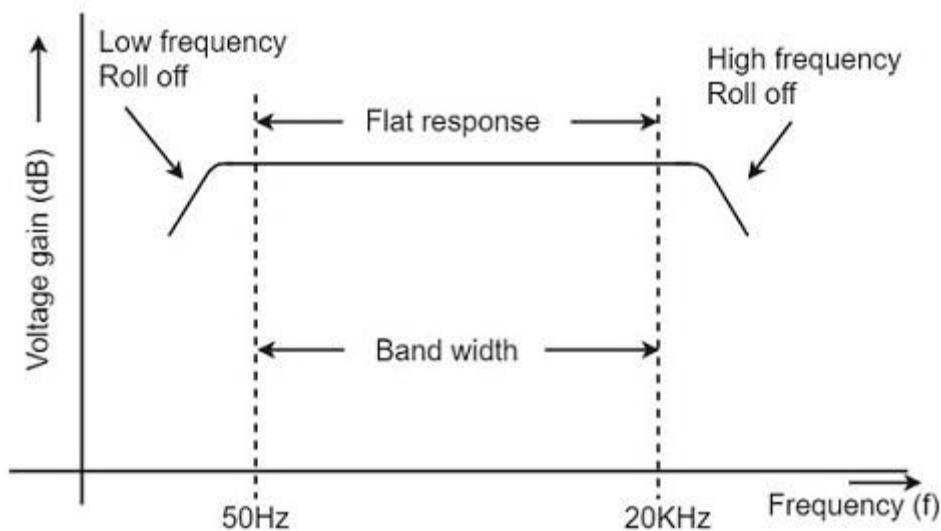
When an AC input signal is applied to the base of first transistor, it gets amplified and appears at the collector load R_L which is then passed through the coupling capacitor C_C to the next stage. This becomes the input of the next stage, whose amplified output again appears across its collector load. Thus the signal is amplified in stage by stage action.

The important point that has to be noted here is that the total gain is less than the product of the gains of individual stages. This is because when a second stage is made to follow the first stage, the **effective load resistance** of the first stage is reduced due to the shunting effect of the input resistance of the second stage. Hence, in a multistage amplifier, only the gain of the last stage remains unchanged.

As we consider a two stage amplifier here, the output phase is same as input. Because the phase reversal is done two times by the two stage CE configured amplifier circuit.

Frequency Response of RC Coupled Amplifier

Frequency response curve is a graph that indicates the relationship between voltage gain and function of frequency. The frequency response of a RC coupled amplifier is as shown in the following graph.



From the above graph, it is understood that the frequency rolls off or decreases for the frequencies below 50 Hz and for the frequencies above 20 KHz. whereas the voltage gain for the range of frequencies between 50 Hz and 20 KHz is constant.

We know that,

$$X_C = \frac{1}{2\pi f C} \quad X_C = \frac{1}{2\pi f C}$$

It means that the capacitive reactance is inversely proportional to the frequency.

At Low frequencies (i.e. below 50 Hz)

The capacitive reactance is inversely proportional to the frequency. At low frequencies, the reactance is quite high. The reactance of input capacitor C_{in} and the coupling capacitor C_C are so high that only small part of the input signal is allowed. The reactance of the emitter bypass capacitor C_E is also very high during low frequencies. Hence it cannot shunt the emitter resistance effectively. With all these factors, the voltage gain rolls off at low frequencies.

At High frequencies (i.e. above 20 KHz)

Again considering the same point, we know that the capacitive reactance is low at high frequencies. So, a capacitor behaves as a short circuit, at high frequencies. As a result of this, the loading effect of the next stage increases, which reduces the voltage gain. Along with this, as the capacitance of emitter diode decreases, it increases the base current of the transistor due to which the current gain (β) reduces. Hence the voltage gain rolls off at high frequencies.

At Mid-frequencies (i.e. 50 Hz to 20 KHz)

The voltage gain of the capacitors is maintained constant in this range of frequencies, as shown in figure. If the frequency increases, the reactance of the capacitor C_C decreases which tends to increase the gain. But this lower capacitance reactive increases the loading effect of the next stage by which there is a reduction in gain.

Due to these two factors, the gain is maintained constant.

Advantages of RC Coupled Amplifier

The following are the advantages of RC coupled amplifier.

- The frequency response of RC amplifier provides constant gain over a wide frequency range, hence most suitable for audio applications.
- The circuit is simple and has lower cost because it employs resistors and capacitors which are cheap.
- It becomes more compact with the upgrading technology.

Disadvantages of RC Coupled Amplifier

The following are the disadvantages of RC coupled amplifier.

- The voltage and power gain are low because of the effective load resistance.
- They become noisy with age.
- Due to poor impedance matching, power transfer will be low.

Applications of RC Coupled Amplifier

The following are the applications of RC coupled amplifier.

- They have excellent audio fidelity over a wide range of frequency.
- Widely used as Voltage amplifiers
- Due to poor impedance matching, RC coupling is rarely used in the final stages.

We have observed that the main drawback of RC coupled amplifier is that the effective load resistance gets reduced. This is because, the input impedance of an amplifier is low, while its output impedance is high.

When they are coupled to make a multistage amplifier, the high output impedance of one stage comes in parallel with the low input impedance of next stage. Hence, effective load resistance is decreased. This problem can be overcome by a **transformer coupled amplifier**.

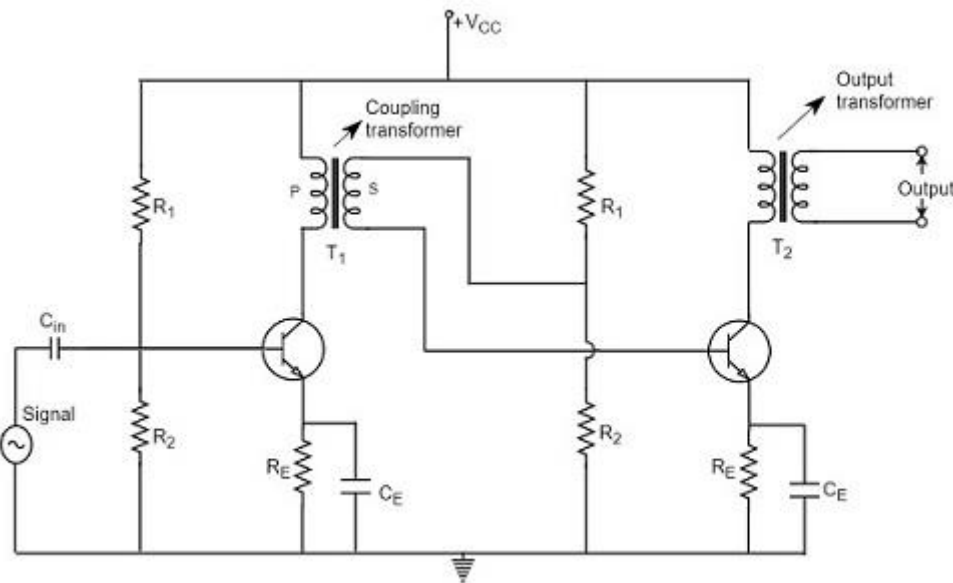
In a transformer-coupled amplifier, the stages of amplifier are coupled using a transformer. Let us go into the constructional and operational details of a transformer coupled amplifier.

Construction of Transformer Coupled Amplifier

The amplifier circuit in which, the previous stage is connected to the next stage using a coupling transformer, is called as Transformer coupled amplifier.

The coupling transformer T_1 is used to feed the output of 1st stage to the input of 2nd stage. The collector load is replaced by the primary winding of the transformer. The secondary winding is connected between the potential divider and the base of 2nd stage, which provides the input to the 2nd stage. Instead of coupling capacitor like in RC coupled amplifier, a transformer is used for coupling any two stages, in the transformer coupled amplifier circuit.

The figure below shows the circuit diagram of transformer coupled amplifier.



The potential divider network R_1 and R_2 and the resistor R_e together form the biasing and stabilization network. The emitter by-pass capacitor C_e offers a low reactance path to the signal. The resistor R_L is used as a load impedance. The input capacitor C_{in} present at the initial stage of the amplifier couples AC signal to the base of the transistor. The capacitor C_C is the coupling capacitor that connects two stages and prevents DC interference between the stages and controls the shift of operating point.

Operation of Transformer Coupled Amplifier

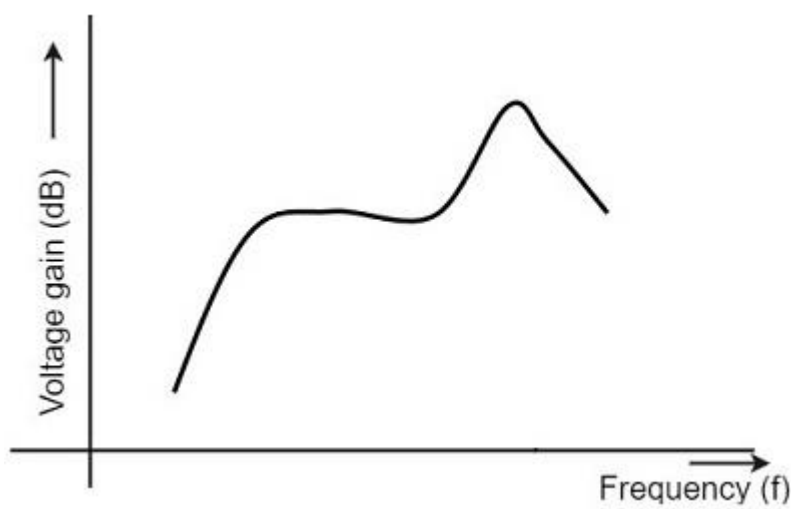
When an AC signal is applied to the input of the base of the first transistor then it gets amplified by the transistor and appears at the collector to which the primary of the transformer is connected.

The transformer which is used as a coupling device in this circuit has the property of impedance changing, which means the low resistance of a stage (or load) can be reflected as a high load resistance to the previous stage. Hence the voltage at the primary is transferred according to the turns ratio of the secondary winding of the transformer.

This transformer coupling provides good impedance matching between the stages of amplifier. The transformer coupled amplifier is generally used for power amplification.

Frequency Response of Transformer Coupled Amplifier

The figure below shows the frequency response of a transformer coupled amplifier. The gain of the amplifier is constant only for a small range of frequencies. The output voltage is equal to the collector current multiplied by the reactance of primary.



At low frequencies, the reactance of primary begins to fall, resulting in decreased gain. At high frequencies, the capacitance between turns of windings acts as a bypass condenser to reduce the output voltage and hence gain.

So, the amplification of audio signals will not be proportionate and some distortion will also get introduced, which is called as **Frequency distortion**.

Advantages of Transformer Coupled Amplifier

The following are the advantages of a transformer coupled amplifier –

- An excellent impedance matching is provided.
- Gain achieved is higher.
- There will be no power loss in collector and base resistors.
- Efficient in operation.

Disadvantages of Transformer Coupled Amplifier

The following are the disadvantages of a transformer coupled amplifier –

- Though the gain is high, it varies considerably with frequency. Hence a poor frequency response.
- Frequency distortion is higher.
- Transformers tend to produce hum noise.
- Transformers are bulky and costly.

Applications

The following are the applications of a transformer coupled amplifier –

- Mostly used for impedance matching purposes.
- Used for Power amplification.
- Used in applications where maximum power transfer is needed.

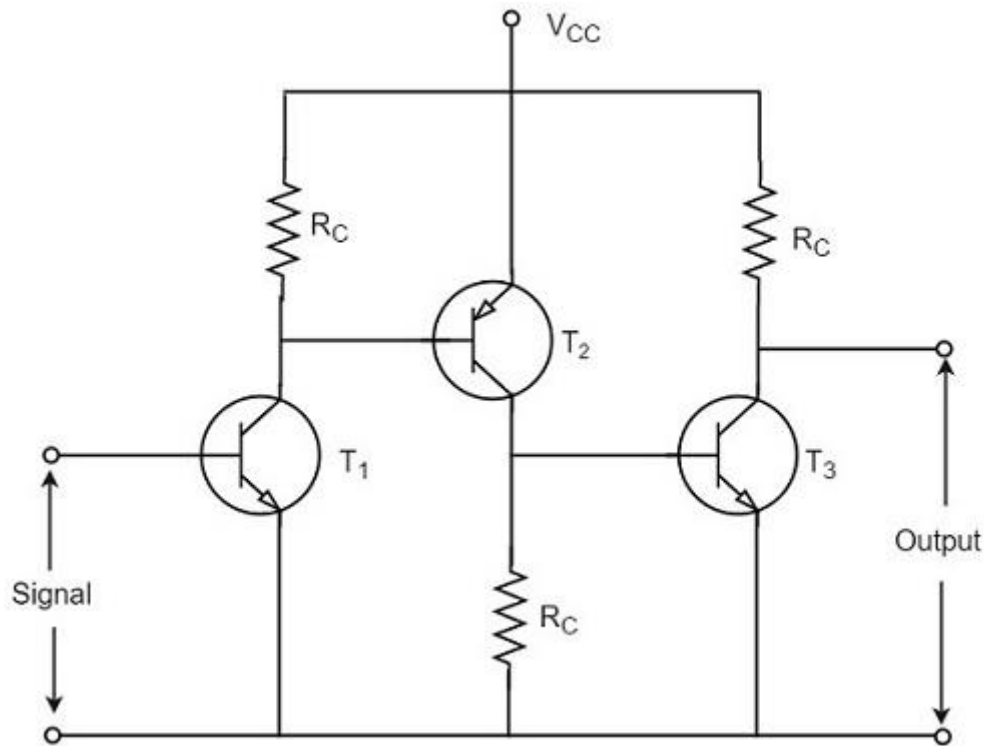
The other type of coupling amplifier is the direct coupled amplifier, which is especially used to amplify lower frequencies, such as amplifying photo-electric current or thermo-couple current or so.

Direct Coupled Amplifier

As no coupling devices are used, the coupling of the amplifier stages is done directly and hence called as **Direct coupled amplifier**.

Construction

The figure below indicates the three stage direct coupled transistor amplifier. The output of first stage transistor T_1 is connected to the input of second stage transistor T_2 .



The transistor in the first stage will be an NPN transistor, while the transistor in the next stage will be a PNP transistor and so on. This is because, the variations in one transistor tend to cancel the variations in the other. The rise in the collector current and the variation in β of one transistor gets cancelled by the decrease in the other.

Operation

The input signal when applied at the base of transistor T_1 , it gets amplified due to the transistor action and the amplified output appears at the collector resistor R_C of transistor T_1 . This output is applied to the base of transistor T_2 which further amplifies the signal. In this way, a signal is amplified in a direct coupled amplifier circuit.

Advantages

The advantages of direct coupled amplifier are as follows.

- The circuit arrangement is simple because of minimum use of resistors.
- The circuit is of low cost because of the absence of expensive coupling devices.

Disadvantages

The disadvantages of direct coupled amplifier are as follows.

- It cannot be used for amplifying high frequencies.

- The operating point is shifted due to temperature variations.

Applications

The applications of direct coupled amplifier are as follows.

- Low frequency amplifications.
- Low current amplifications.

Comparisons

Let us try to compare the characteristics of different types of coupling methods discussed till now.

| S.No | Particular | RC Coupling | Transformer Coupling | Direct Coupling |
|------|--------------------|------------------------------------|-------------------------|--|
| 1 | Frequency response | Excellent in audio frequency range | Poor | Best |
| 2 | Cost | Less | More | Least |
| 3 | Space and Weight | Less | More | Least |
| 4 | Impedance matching | Not good | Excellent | Good |
| 5 | Use | For voltage amplification | For Power amplification | For amplifying extremely low frequencies |

Emitter follower and darlington amplifier are the most common examples for feedback amplifiers. These are the mostly used ones with a number of applications.

Emitter Follower

Emitter follower circuit has a prominent place in feedback amplifiers. Emitter follower is a case of negative current feedback circuit. This is mostly used as a last stage amplifier in signal generator circuits.

The important features of Emitter Follower are –

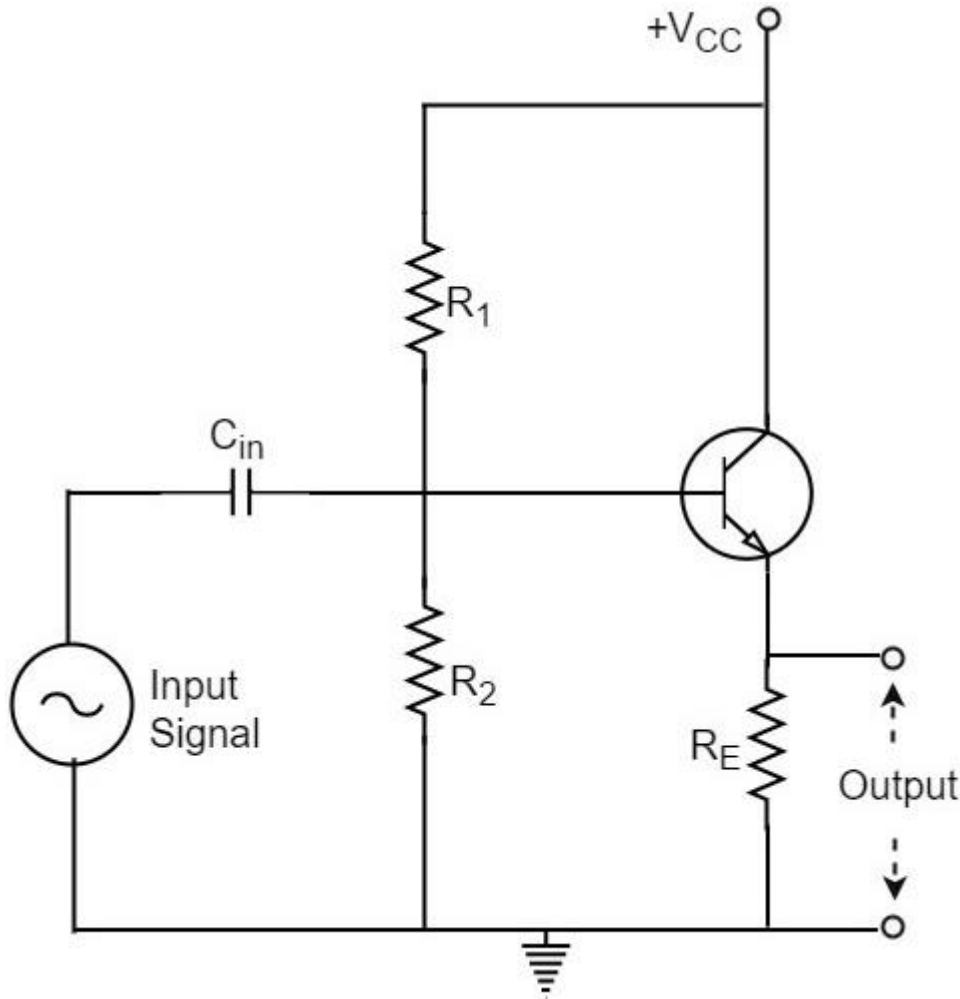
- It has high input impedance
- It has low output impedance
- It is ideal circuit for impedance matching

All these ideal features allow many applications for the emitter follower circuit. This is a current amplifier circuit that has no voltage gain.

Construction

The constructional details of an emitter follower circuit are nearly similar to a normal amplifier. The main difference is that the load R_L is absent at the collector terminal, but present at the emitter terminal of the circuit. Thus the output is taken from the emitter terminal instead of collector terminal.

The biasing is provided either by base resistor method or by potential divider method. The following figure shows the circuit diagram of an Emitter Follower.



Operation

The input signal voltage applied between base and emitter, develops an output voltage V_o across R_E , which is in the emitter section. Therefore,

$$V_o = I_E R_E \quad V_o = I_E R_E$$

The whole of this output current is applied to the input through feedback. Hence,

$$V_f = V_o \quad V_f = V_o$$

As the output voltage developed across R_L is proportional to the emitter current, this emitter follower circuit is a current feedback circuit. Hence,

$$\beta = V_f / V_o = 1 \quad \beta = V_f / V_o = 1$$

It is also noted that the input signal voltage to the transistor ($= V_i$) is equal to the difference of V_s and V_o i.e.,

$$V_i = V_s - V_o$$

Hence the feedback is negative.

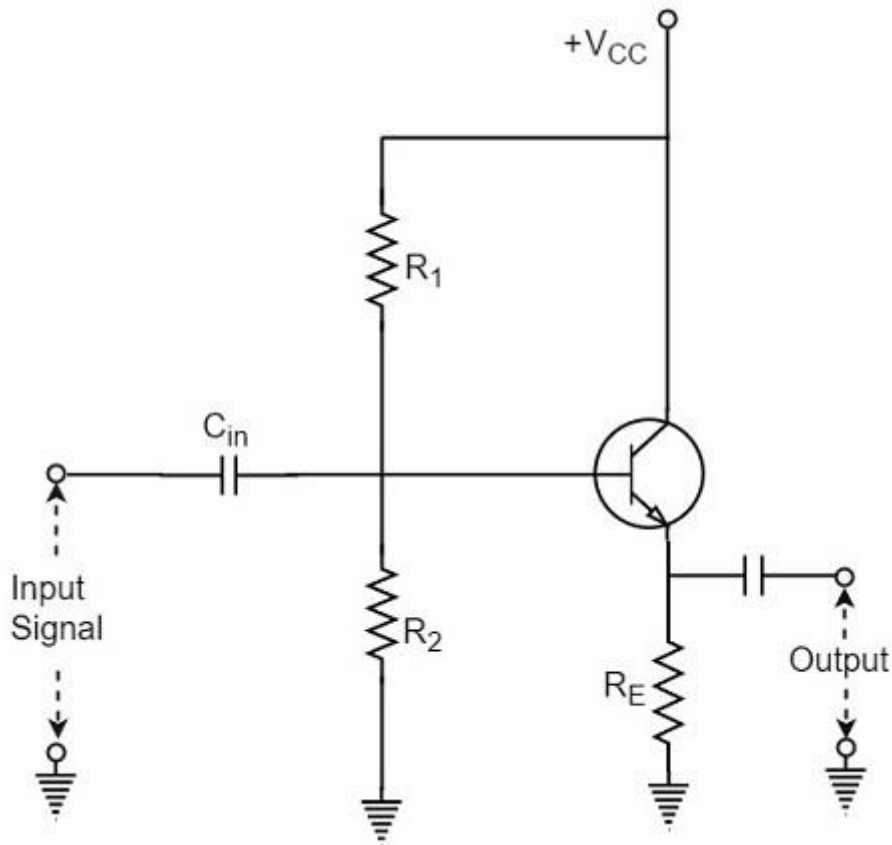
Characteristics

The major characteristics of the emitter follower are as follows –

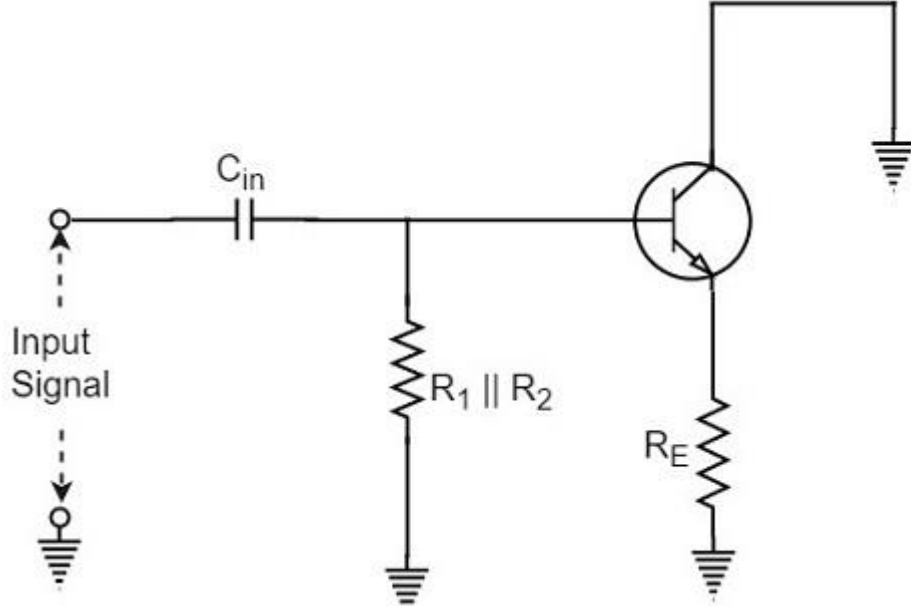
- No voltage gain. In fact, the voltage gain is nearly 1.
- Relatively high current gain and power gain.
- High input impedance and low output impedance.
- Input and output ac voltages are in phase.

Voltage Gain of Emitter Follower

As the Emitter Follower circuit is a prominent one, let us try to get the equation for the voltage gain of an emitter follower circuit. Our Emitter Follower circuit looks as follows –



If an AC equivalent circuit of the above circuit is drawn, it would look like the below one, as the emitter by pass capacitor is absent.



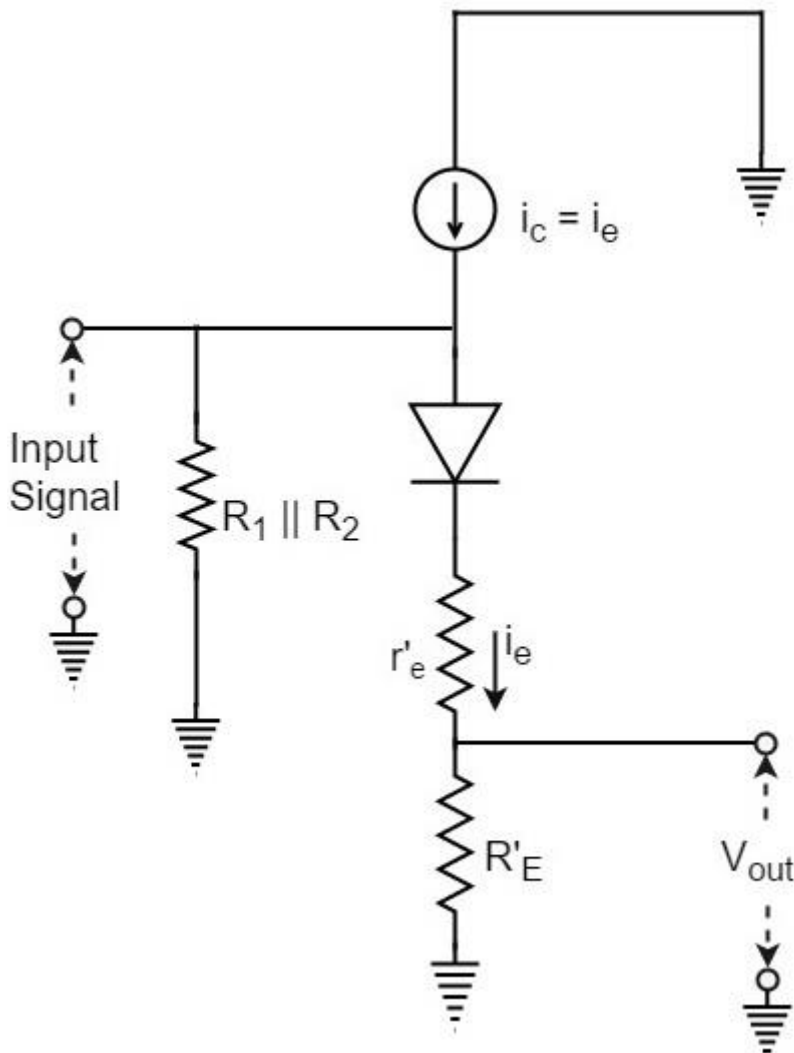
The AC resistance r_E of the emitter circuit is given by

$$r_E = r'_E + R_E$$

Where

$$r'_E = \frac{25\text{mV}}{I_E}$$

In order to find the voltage gain of the amplifier, the above figure can be replaced by the following figure.



Note that input voltage is applied across the ac resistance of the emitter circuit i.e., $(r'_E + R_E)$. Assuming the emitter diode to be ideal, the output voltage V_{out} will be

$$V_{out} = i_e R_E \quad V_{out} = i_e R_E$$

Input voltage V_{in} will be

$$V_{in} = i_e (r'_e + R_E) \quad V_{in} = i_e (r'_e + R_E)$$

Therefore, the Voltage Gain of emitter follower is

$$A_V = \frac{V_{out}}{V_{in}} = \frac{i_e R_E}{i_e (r'_e + R_E)} = \frac{R_E}{r'_e + R_E} \quad A_V = \frac{V_{out}}{V_{in}} = \frac{i_e R_E}{i_e (r'_e + R_E)} = \frac{R_E}{r'_e + R_E}$$

Or

$$A_V = \frac{R_E}{r'_e + R_E} \quad A_V = \frac{R_E}{r'_e + R_E}$$

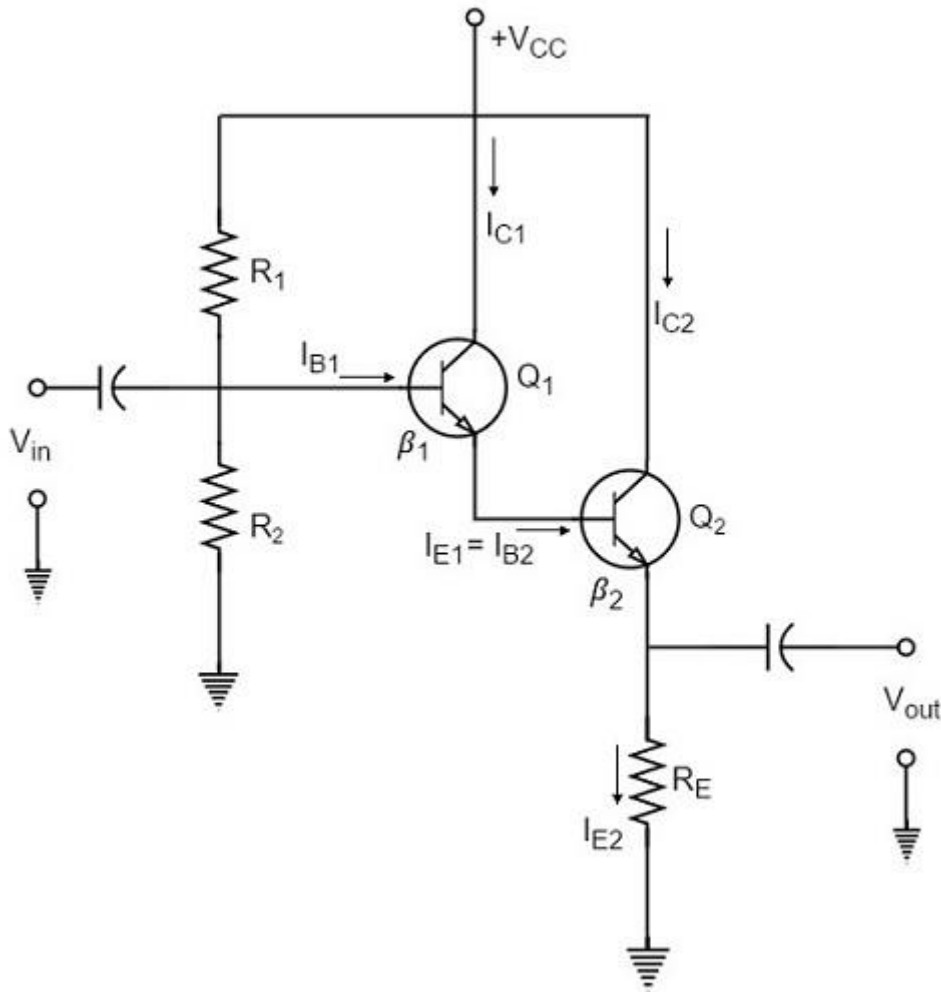
In most practical applications,

$$R_E \gg r'_e \quad R_E \gg r'_e$$

So, $A_V \approx 1$. In practice, the voltage gain of an emitter follower is between 0.8 and 0.999.

Darlington Amplifier

The emitter follower circuit which was just discussed lacks to meet the requirements of the circuit current gain (A_i) and the input impedance (Z_i). In order to achieve some increase in the overall values of circuit current gain and input impedance, two transistors are connected as shown in the following circuit diagram, which is known as **Darlington** configuration.



As shown in the above figure, the emitter of the first transistor is connected to the base of the second transistor. The collector terminals of both the transistors are connected together.

Biasing Analysis

Because of this type of connection, the emitter current of the first transistor will also be the base current of the second transistor. Therefore, the current gain of the pair is equal to the product of individual current gains i.e.,

$$\beta = \beta_1 \beta_2$$

A high current gain is generally achieved with a minimum number of components.

As two transistors are used here, two V_{BE} drops are to be considered. The biasing analysis is otherwise similar for one transistor.

Voltage across R_2 ,

$$V_2 = V_{CC} \frac{R_1}{R_1 + R_2}$$

Voltage across R_E ,

$$V_E = V_2 - 2V_{BE}$$

Current through R_E ,

$$I_{E2} = \frac{V_E}{R_E}$$

Since the transistors are directly coupled,

$$I_{E1} = I_{B2}$$

Now

$$I_{B2} = \frac{I_{E2}}{\beta_2}$$

Therefore

$$I_{E1} = \beta_1 I_{B2}$$

Which means

$$I_{E1} = \beta_1 \beta_2 I_{E2}$$

We have

$$I_{E1} = \beta_1 I_{B1} \text{ since } I_{E1} \cong I_{C1}$$

Hence, as

$$I_{E2} = \frac{I_{E1}}{\beta_1 \beta_2}$$

We can write

$$I_{E2} = \beta_1 \beta_2 I_{B1}$$

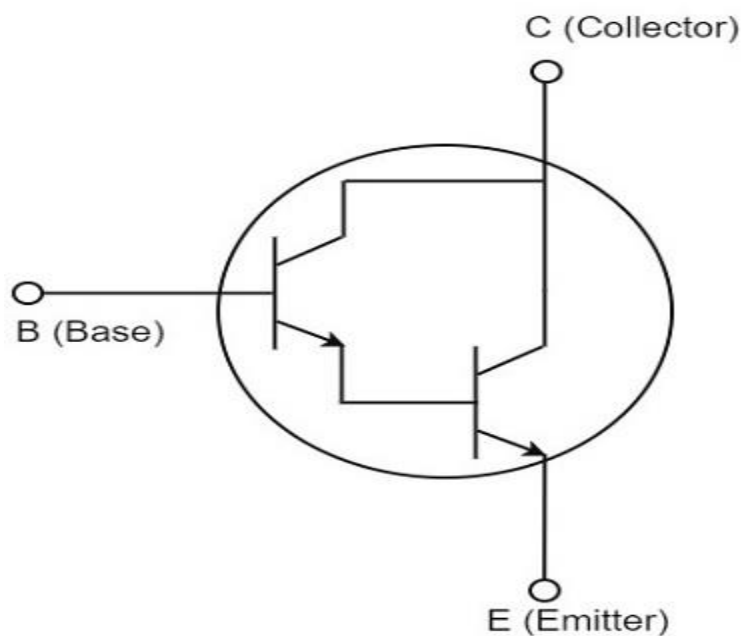
Therefore, Current Gain can be given as

$$\beta = \frac{I_{E2}}{I_{B1}} = \beta_1 \beta_2$$

Input impedance of the darlington amplifier is

$$Z_{in} = \beta_1 \beta_2 R_E \dots \text{ neglecting } r'_e$$

In practice, these two transistors are placed in a single transistor housing and the three terminals are taken out of the housing as shown in the following figure.



This three terminal device can be called as **Darlington transistor**. The darlington transistor acts like a single transistor that has high current gain and high input impedance.

Characteristics

The following are the important characteristics of Darlington amplifier.

- Extremely high input impedance ($M\Omega$).
- Extremely high current gain (several thousands).
- Extremely low output impedance (a few Ω).

Since the characteristics of the Darlington amplifier are basically the same as those of the emitter follower, the two circuits are used for similar applications.

Till now we have discussed amplifiers based on positive feedback. The negative feedback in transistor circuits is helpful in the working of oscillators. The topic of oscillators is entirely covered in Oscillators tutorial.

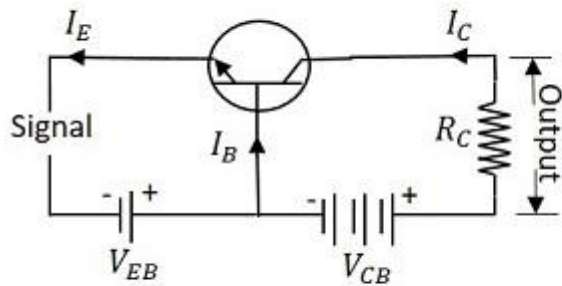
A Transistor has 3 terminals, the emitter, the base and the collector. Using these 3 terminals the transistor can be connected in a circuit with one terminal common to both input and output in a 3 different possible configurations.

The three types of configurations are **Common Base**, **Common Emitter** and **Common Collector** configurations. In every configuration, the emitter junction is forward biased and the collector junction is reverse biased.

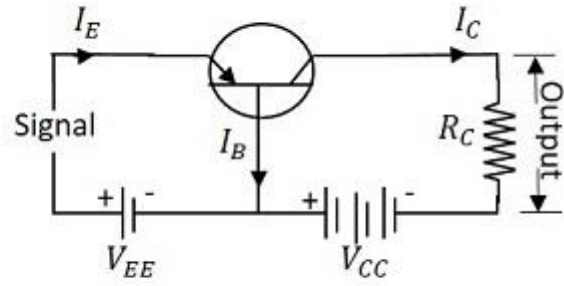
Common Base Configuration

The name itself implies that the Base terminal is taken as common terminal for both input and output of the transistor. The common base connection for both NPN and PNP transistors is as shown in the following figure.

Common Base Connection



Using NPN transistor



Using PNP transistor

For the sake of understanding, let us consider NPN transistor in CB configuration. When the emitter voltage is applied, as it is forward biased, the electrons from the negative terminal repel the emitter electrons and current flows through the emitter and base to the collector to contribute collector current. The collector voltage V_{CB} is kept constant throughout this.

In the CB configuration, the input current is the emitter current I_E and the output current is the collector current I_C .

Current Amplification Factor α

The ratio of change in collector current ΔI_C to the change in emitter current ΔI_E when collector voltage V_{CB} is kept constant, is called as **Current amplification factor**. It is denoted by α .

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \text{ at constant } V_{CB} \quad \alpha = \frac{\Delta I_C}{\Delta I_E} \text{ at constant } V_{CB}$$

Expression for Collector current

With the idea above, let us try to draw some expression for collector current. Along with the emitter current flowing, there is some amount of base current I_B which flows through the base terminal due to electron hole recombination. As collector-base junction is reverse biased, there is another current which is flown due to minority charge carriers. This is the leakage current which can be understood as $I_{leakage}$. This is due to minority charge carriers and hence very small.

The emitter current that reaches the collector terminal is

$$\alpha I_E$$

Total collector current

$$I_C = \alpha I_E + I_{leakage} \quad I_C = \alpha I_E + I_{leakage}$$

If the emitter-base voltage $V_{EB} = 0$, even then, there flows a small leakage current, which can be termed as I_{CBO} collector-base current without output open collector-base current without output open.

The collector current therefore can be expressed as

$$I_C = \alpha I_E + I_{CBO} \quad I_C = \alpha I_E + I_{CBO}$$

$$I_E = I_C + I_B \quad I_E = I_C + I_B$$

$$I_C = \alpha (I_C + I_B) + I_{CBO} \quad I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO} \quad I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha I_B + I_{CBO}}{1 - \alpha} \quad I_C = \frac{\alpha I_B + I_{CBO}}{1 - \alpha}$$

$$I_C = \frac{\alpha I_B + I_{CBO}}{1 - \alpha} \quad I_C = \frac{\alpha I_B + I_{CBO}}{1 - \alpha}$$

Hence the above derived is the expression for collector current. The value of collector current depends on base current and leakage current along with the current amplification factor of that transistor in use.

Characteristics of CB configuration

- This configuration provides voltage gain but no current gain.
- Being V_{CB} constant, with a small increase in the Emitter-base voltage V_{EB} , Emitter current I_E gets increased.
- Emitter Current I_E is independent of Collector voltage V_{CB} .
- Collector Voltage V_{CB} can affect the collector current I_C only at low voltages, when V_{EB} is kept constant.
- The input resistance r_i is the ratio of change in emitter-base voltage ΔV_{EB} to the change in emitter current ΔI_E at constant collector base voltage V_{CB} .

$$r_i = \frac{\Delta V_{EB}}{\Delta I_E} \text{ at constant } V_{CB}$$

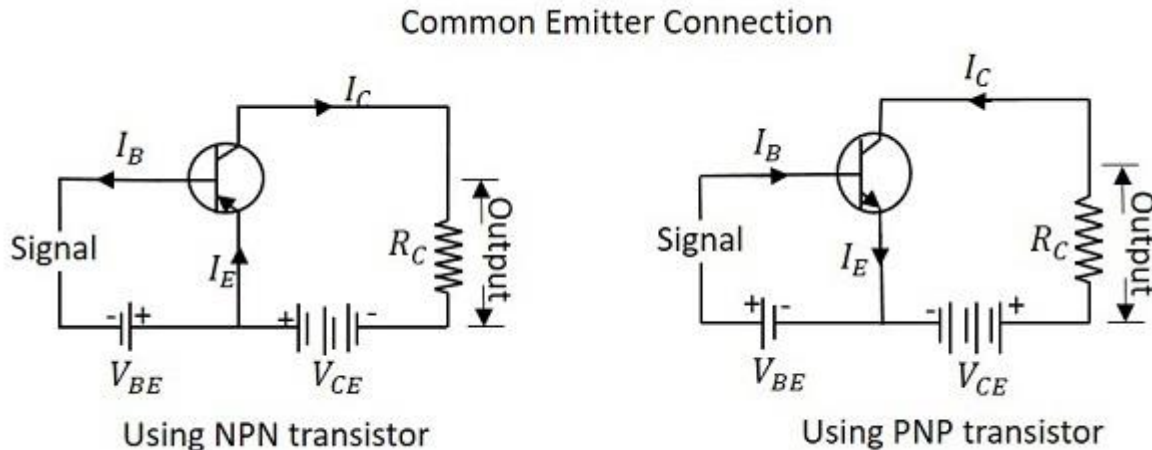
- As the input resistance is of very low value, a small value of V_{EB} is enough to produce a large current flow of emitter current I_E .
- The output resistance r_o is the ratio of change in the collector base voltage ΔV_{CB} to the change in collector current ΔI_C at constant emitter current I_E .

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C} \text{ at constant } I_E$$

- As the output resistance is of very high value, a large change in V_{CB} produces a very little change in collector current I_C .
- This Configuration provides good stability against increase in temperature.
- The CB configuration is used for high frequency applications.

Common Emitter CECE Configuration

The name itself implies that the **Emitter** terminal is taken as common terminal for both input and output of the transistor. The common emitter connection for both NPN and PNP transistors is as shown in the following figure.



Just as in CB configuration, the emitter junction is forward biased and the collector junction is reverse biased. The flow of electrons is controlled in the same manner. The input current is the base current I_B and the output current is the collector current I_C here.

Base Current Amplification factor β

The ratio of change in collector current ΔI_C to the change in base current ΔI_B is known as **Base Current Amplification Factor**. It is denoted by β

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

Relation between β and α

Let us try to derive the relation between base current amplification factor and emitter current amplification factor.

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

$$I_E = I_B + I_C$$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

We can write

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C}$$

Dividing by

$$\beta = \frac{\Delta I_C \Delta I_E}{\Delta I_E - \Delta I_C}$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

We have

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

Therefore,

$$\beta = \frac{\alpha}{1 - \alpha}$$

From the above equation, it is evident that, as α approaches 1, β reaches infinity.

Hence, **the current gain in Common Emitter connection is very high**. This is the reason this circuit connection is mostly used in all transistor applications.

Expression for Collector Current

In the Common Emitter configuration, I_B is the input current and I_C is the output current.

We know

$$I_E = I_B + I_C$$

And

$$I_C = \alpha I_E + I_{CBO}$$

$$= \alpha (I_B + I_C) + I_{CBO}$$

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha I_B + I_{CBO}}{1 - \alpha}$$

If base circuit is open, i.e. if $I_B = 0$,

The collector emitter current with base open is I_{CEO}

$$I_{CE0} = (1 - \alpha) I_{CB0} \quad I_{CE0} = (1 - \alpha) I_{CB0}$$

Substituting the value of this in the previous equation, we get

$$I_C = \alpha I_B + I_{CE0} \quad I_C = \alpha I_B + I_{CE0}$$

$$I_C = \beta I_B + I_{CE0} \quad I_C = \beta I_B + I_{CE0}$$

Hence the equation for collector current is obtained.

Knee Voltage

In CE configuration, by keeping the base current I_B constant, if V_{CE} is varied, I_C increases nearly to 1V of V_{CE} and stays constant thereafter. This value of V_{CE} up to which collector current I_C changes with V_{CE} is called the **Knee Voltage**. The transistors while operating in CE configuration, they are operated above this knee voltage.

Characteristics of CE Configuration

- This configuration provides good current gain and voltage gain.
- Keeping V_{CE} constant, with a small increase in V_{BE} the base current I_B increases rapidly than in CB configurations.
- For any value of V_{CE} above knee voltage, I_C is approximately equal to βI_B .
- The input resistance r_i is the ratio of change in base emitter voltage ΔV_{BE} to the change in base current ΔI_B at constant collector emitter voltage V_{CE} .

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at constant } V_{CE} \quad r_i = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at constant } V_{CE}$$

- As the input resistance is of very low value, a small value of V_{BE} is enough to produce a large current flow of base current I_B .
- The output resistance r_o is the ratio of change in collector emitter voltage ΔV_{CE} to the change in collector current ΔI_C at constant I_B .

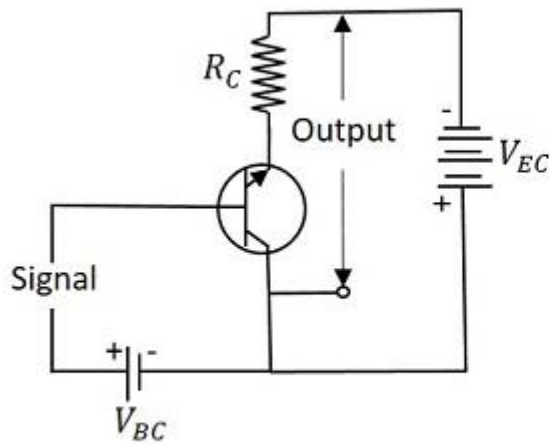
$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B \quad r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B$$

- As the output resistance of CE circuit is less than that of CB circuit.
- This configuration is usually used for bias stabilization methods and audio frequency applications.

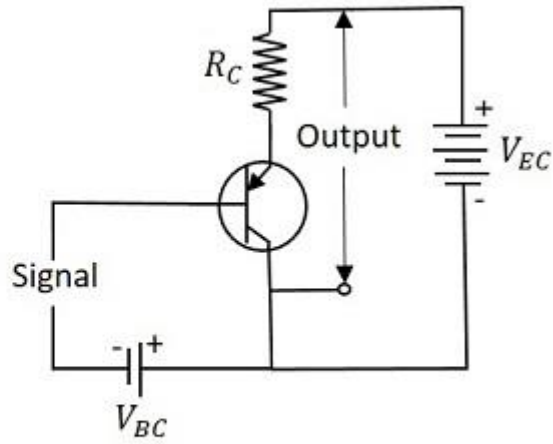
Common Collector CCCC Configuration

The name itself implies that the **Collector** terminal is taken as common terminal for both input and output of the transistor. The common collector connection for both NPN and PNP transistors is as shown in the following figure.

Common Collector Connection



Using NPN transistor



Using PNP transistor

Just as in CB and CE configurations, the emitter junction is forward biased and the collector junction is reverse biased. The flow of electrons is controlled in the same manner. The input current is the base current I_B and the output current is the emitter current I_E here.

Current Amplification Factor γ

The ratio of change in emitter current ΔI_E to the change in base current ΔI_B is known as **Current Amplification factor** in common collector CCCC configuration. It is denoted by γ .

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

- The current gain in CC configuration is same as in CE configuration.
- The voltage gain in CC configuration is always less than 1.

Relation between γ and α

Let us try to draw some relation between γ and α

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

$$I_E = I_B + I_C$$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

Substituting the value of I_B , we get

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Dividing by ΔI_E

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C} \Rightarrow \gamma = \frac{1}{1 - \frac{\Delta I_C}{\Delta I_E}}$$

$$1 - \alpha$$

$$\gamma = \frac{1}{1 - \alpha}$$

Expression for collector current

We know

$$I_C = \alpha I_E + I_{CBO} \quad I_C = \alpha I_E + I_{CBO}$$

$$I_E = I_B + I_C = I_B + (\alpha I_E + I_{CBO}) \quad I_E = I_B + I_C = I_B + (\alpha I_E + I_{CBO})$$

$$I_E(1 - \alpha) = I_B + I_{CBO} \quad I_E(1 - \alpha) = I_B + I_{CBO}$$

$$I_E = \frac{I_B + I_{CBO}}{1 - \alpha} \quad I_E = \frac{I_B + I_{CBO}}{1 - \alpha}$$

$$I_C \cong I_E = (\beta + 1)I_B + (\beta + 1)I_{CBO} \quad I_C \cong I_E = (\beta + 1)I_B + (\beta + 1)I_{CBO}$$

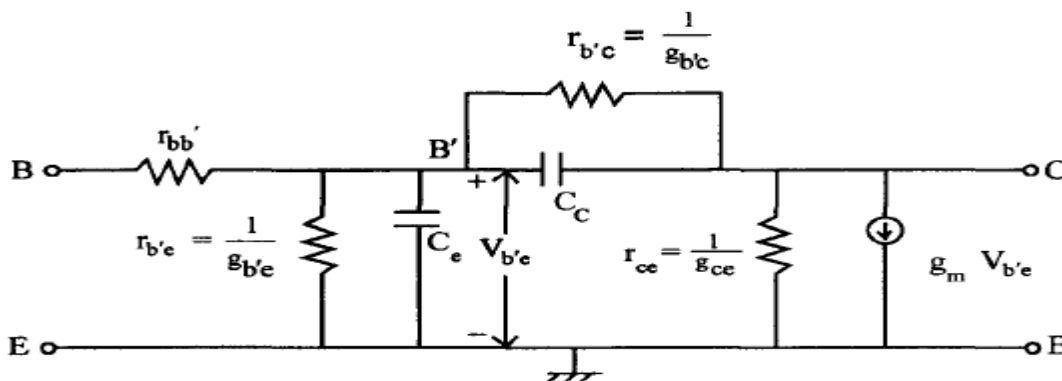
The above is the expression for collector current.

Characteristics of CC Configuration

- This configuration provides current gain but no voltage gain.
- In CC configuration, the input resistance is high and the output resistance is low.
- The voltage gain provided by this circuit is less than 1.
- The sum of collector current and base current equals emitter current.
- The input and output signals are in phase.
- This configuration works as non-inverting amplifier output.
- This circuit is mostly used for impedance matching. That means, to drive a low impedance load from a high impedance source.

Hybrid - π Common Emitter Transconductance Model

For Transconductance amplifier circuits Common Emitter configuration is preferred. Why? Because for Common Collector ($h_{rc} < 1$). For Common Collector Configuration, voltage gain $A_v < 1$. So even by cascading you can't increase voltage gain. For Common Base, current gain is $h_{ib} < 1$. Overall voltage gain is less than 1. For Common Emitter, $h_{re} \gg 1$. Therefore Voltage gain can be increased by cascading Common Emitter stage. So Common Emitter configuration is widely used. The Hybrid- π or Giacoletto Model for the Common Emitter amplifier circuit (single stage) is as shown below.



Analysis of this circuit gives satisfactory results at all frequencies not only at high frequencies but also at low frequencies. All the parameters are assumed to be independent of frequency.

Where B' = internal node in base
 $r_{bb'}$ = Base spreading resistance
 $r_{b'e}$ = Internal base node to emitter resistance
 r_{ce} = collector to emitter resistance
 C_e = Diffusion capacitance of emitter base junction
 $r_{b'c}$ = Feedback resistance from internal base node to collector
node g_m = Transconductance
 C_C = transition or space charge capacitance of base collector junction

Circuit Components

B' is the internal node of base of the Transconductance amplifier. It is not physically accessible. The base spreading resistance r_{bb} is represented as a lumped parameter between base B and internal node B' . $g_m V_{b'e}$ is a current generator. $V_{b'e}$ is the input voltage across the emitter junction. If $V_{b'e}$ increases, more carriers are injected into the base of the transistor. So the increase in the number of carriers is proportional to $V_{b'e}$. This results in small signal current since we are taking into account changes in $V_{b'e}$. This effect is represented by the current generator $g_m V_{b'e}$. This represents the current that results because of the changes in $V_{b'e}$ when C is shorted to E .

When the number of carriers injected into the base increase, base recombination also increases. So this effect is taken care of by $g_{b'e}$. As recombination increases, base current increases. Minority carrier storage in the base is represented by C_e the diffusion capacitance.

According to Early Effect, the change in voltage between Collector and Emitter changes the base width. Base width will be modulated according to the voltage variations between Collector and Emitter. When base width changes, the minority carrier concentration in base changes. Hence the current which is proportional to carrier concentration also changes. I_E changes and I_C changes. This feedback effect [I_E on input side, I_C on output side] is taken into account by connecting $g_{b'e}$ between B' , and C . The conductance between Collector and Base is g_{ce} . C_C represents the collector junction barrier capacitance.

Hybrid - n Parameter Values

Typical values of the hybrid-n parameter at $I_C = 1.3 \text{ mA}$ are as follows:

$$g_m = 50 \text{ mA/v}$$

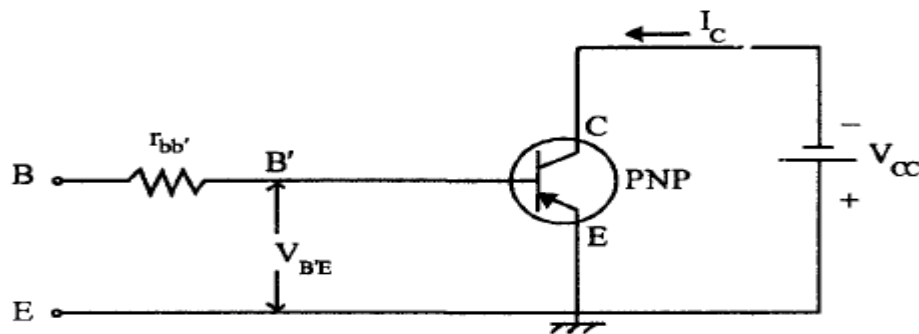
$$\begin{aligned}
 r_{bb'} &= 100 \Omega \\
 r_{b'e} &= 1 \text{ k}\Omega \\
 r_{ee} &= 80 \text{ k}\Omega \\
 C_c &= 3 \text{ pf} \\
 C_e &= 100 \text{ pf} \\
 r_{b'c} &= 4 \text{ M}\Omega
 \end{aligned}$$

These values depend upon:

1. Temperature
2. Value of I_C

Determination of Hybrid- π Conductances

1. Trans conductance or Mutual Conductance (g_m)



The above figure shows PNP transistor amplifier in Common Emitter configuration for AC purpose, Collector is shorted to Emitter.

$$I_C = I_{C0} - \alpha_0 \cdot I_E$$

I_{C0} opposes I_E . I_E is negative. Hence $I_C = I_{C0} - \alpha_0 I_E$ α_0 is the normal value of α at room temperature.

In the hybrid - π equivalent circuit, the short circuit current = $g_m V_{b'e}$

Here only transistor is considered, and other circuit elements like resistors, capacitors etc are not considered.

$$g_m = \left. \frac{\partial I_C}{\partial V_{b'e}} \right|_{V_{CE} = K}$$

Differentiate (1) with respect to $V_{b'e}$ partially. I_{C0} is constant

$$g_m = 0 - \alpha_0 \frac{\partial I_E}{\partial V_{b'e}}$$

For a PNP transistor, $V_{b'e} = -V_E$ Since, for PNP transistor, base is n-type. So negative voltage is given

$$g_m = \alpha_0 \frac{\partial I_E}{\partial V_E}$$

If the emitter diode resistance is r_e then

$$r_e = \frac{\partial V_E}{\partial I_E}$$

$$g_m = \frac{\alpha_0}{r_e}$$

$$r = \frac{\eta \cdot V_T}{I} \quad \eta = 1, \quad I = I_E \quad r = \frac{V_T}{I_E}$$

$$g_m = \frac{\alpha_0 \cdot I_E}{V_T} \quad \alpha_0 \simeq 1, \quad I_E \simeq I_C$$

$$I_E = I_{C0} - I_C$$

$$g_m = \frac{I_{C0} - I_C}{V_T}$$

Neglect I_{C0}

$$g_m = \frac{|I_C|}{V_T}$$

g_m is directly proportional to I_C is also inversely proportional to T . For PNP transistor, I_C is negative

$$g_m = \frac{-I_C}{V_T}$$

At room temperature i.e. $T=300^0\text{K}$

$$g_m = \frac{|I_C|}{26}, I_C \text{ is in mA.}$$

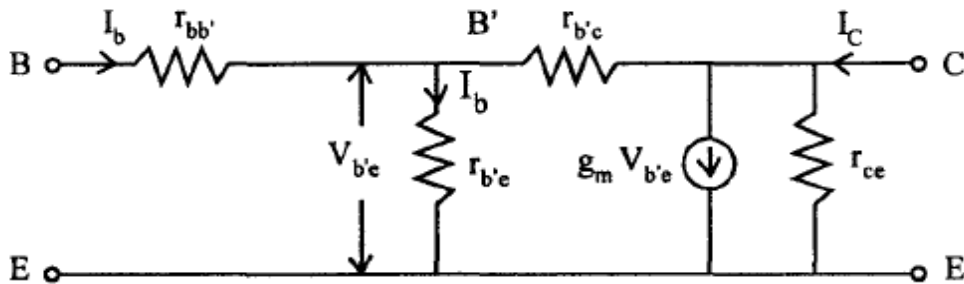
If $I_C = 1.3 \text{ mA}, g_m = 0.05 \text{ A/V}$

If $I_C = 10 \text{ mA}, g_m = 400 \text{ mA/V}$

Input Conductance ($g_{b'e}$):

At low frequencies, capacitive reactance will be very large and can be considered as Open circuit. So in the hybrid- π equivalent circuit which is valid at low frequencies, all the capacitances can be neglected.

The equivalent circuit is as shown in Fig.



The value of $r_{b'c} \gg r_{b'e}$ (Since Collector Base junction is Reverse Biased) So I_b flows into $r_{b'e}$ only. [This is I_b' ($I_E - I_b$) will go to collector junction]

$$V_{b'e} \simeq I_b \cdot r_{b'e}$$

The short circuit collector current,

$$I_C = g_m \cdot V_{b'e}; \quad V_{b'e} = I_b \cdot r_{b'e}$$

$$I_C = g_m \cdot I_b \cdot r_{b'e}$$

$$h_{fe} = \left. \frac{I_C}{I_B} \right|_{V_{CE}} = g_m \cdot r_{b'e}$$

$$\boxed{r_{b'e} = \frac{h_{fe}}{g_m}}$$

$$g_m = \frac{|I_C|}{V_T}$$

$$r_{b'e} = \frac{h_{fe} \cdot V_T}{|I_C|}$$

$$g_{b'e} = \boxed{\frac{|I_C|}{h_{fe} V_T}} \quad \text{or} \quad \boxed{\frac{g_m}{h_{fe}}}$$

Feedback Conductance ($g_{b'c}$)

h_{re} = reverse voltage gain, with input open or $I_b = 0$

$h_{re} = V_{b'e}/V_{ce}$ = Input voltage/Output voltage

$$h_{re} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}}$$

[With input open, i.e., $I_b = 0$, V_{ce} is output. So it will get divided between $r_{b'e}$ and $r_{b'c}$ only]

or

$$h_{re} (r_{b'e} + r_{b'c}) = r_{b'e}$$
$$r_{b'e} [1 - h_{re}] = h_{re} r_{b'c}$$

But

$$h_{re} \ll 1$$

\therefore

$$r_{b'e} = h_{re} r_{b'c}; \quad r_{b'c} = \frac{r_{b'e}}{h_{re}}$$

or

$$\boxed{g_{b'c} = h_{re} g_{b'e}} \quad \frac{1}{r_{b'c}} = g_{b'c} = \frac{h_{re}}{r_{b'e}}$$

$$h_{re} = 10^{-4}$$

\therefore

$$r_{b'c} \gg r_{b'e}$$

Base Spreading Resistance ($r_{bb'}$)

The input resistance with the output shorted is h_{ie} . If output is shorted, i.e., Collector and Emitter are joined; $r_{b'e}$ is in parallel with $r_{b'c}$.

$$h_{ie} = r_{bb'} + r_{b'e}$$

$$\boxed{r_{bb'} = h_{ie} - r_{b'e}}$$

$$h_{ie} = r_{bb'} + r_{b'e}$$

$$r_{b'e} = \frac{h_{fe} \cdot V_T}{|I_C|}$$

$$h_{ie} = r_{bb'} + \frac{h_{fe} \cdot V_T}{|I_C|}$$

Output Conductance (g_{ce})

This is the conductance with input open circuited. In h-parameters it is represented as h_{oe} . For $I_b = 0$, we have,

$$I_C = \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'c} + r_{b'e}} + g_m V_{b'e}$$

$$h_{re} = \frac{V_{b'e}}{V_{ce}}$$

$$\therefore V_{b'e} = h_{re} \cdot V_{ce}$$

$$I_C = \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'c} + r_{b'e}} + g_m \cdot h_{re} \cdot V_{ce}$$

$$h_{oe} = \frac{1}{r_{ce}} + \frac{1}{r_{b'c}} + g_m \cdot h_{re}$$

$$= g_{ce} + g_{b'c} + g_m h_{re}$$

$$g_{b'e} = \frac{g_m}{h_{fe}}$$

$$g_m = g_{b'e} \cdot h_{fe}$$

$$h_{re} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}} \approx \frac{r_{b'e}}{r_{b'c}} = \frac{g_{b'c}}{g_{b'e}}$$

$$h_{oe} = g_{ce} + g_{b'c} + g_{b'e} h_{fe} \cdot \frac{g_{b'c}}{g_{b'e}}$$

$$g_{ce} = h_{oe} - (1 + h_{fe}) \cdot g_{b'c}$$

$$h_{fe} \gg 1, 1 + h_{fe} \approx h_{fe}$$

$$\boxed{g_{ce} = h_{oe} - h_{fe} \cdot g_{b'c}}$$

$$g_{b'c} = h_{re} \cdot g_{b'e}$$

$$g_{ce} = h_{oe} - h_{fe} \cdot h_{re} \cdot g_{b'e}$$

Hybrid - π Capacitances

In the hybrid - π equivalent circuit, there are two capacitances, the capacitance between the Collector Base junction is the C_C or $C_{b'e'}$. This is measured with input open i.e., $I_E = 0$, and is specified by the manufacturers as $C_{Ob. 0}$. 0 indicates that input is open. Collector junction is reverse biased.

$$C_C \propto \frac{1}{(V_{CE})^n}$$

$$n = \frac{1}{2} \text{ for abrupt junction}$$

$$= 1/3 \text{ for graded junction.}$$

C_e = Emitter diffusion capacitance C_{De} + Emitter junction capacitance C_{Te}

C_T = Transition capacitance.

C_D = Diffusion capacitance.

$$C_{De} \gg C_{Te}$$

$$C_e \approx C_{De}$$

$C_{De} \propto I_E$ and is independent of Temperature T .

Validity of hybrid- π model

The high frequency hybrid Pi or Giacoletto model of BJT is valid for frequencies less than the unit gain frequency.

High frequency model parameters of a BJT in terms of low frequency hybrid parameters

The main advantage of high frequency model is that this model can be simplified to obtain low frequency model of BJT. This is done by eliminating capacitance's from the high frequency model so that the BJT responds without any significant delay (instantaneously) to the input signal. In practice there will be some delay between the input signal and output signal of BJT which will be very small compared to signal period (1/frequency of input signal) and hence can be neglected. The high frequency model of BJT is simplified at low frequencies and redrawn as shown in the figure below along with the small signal low frequency hybrid model of BJT.

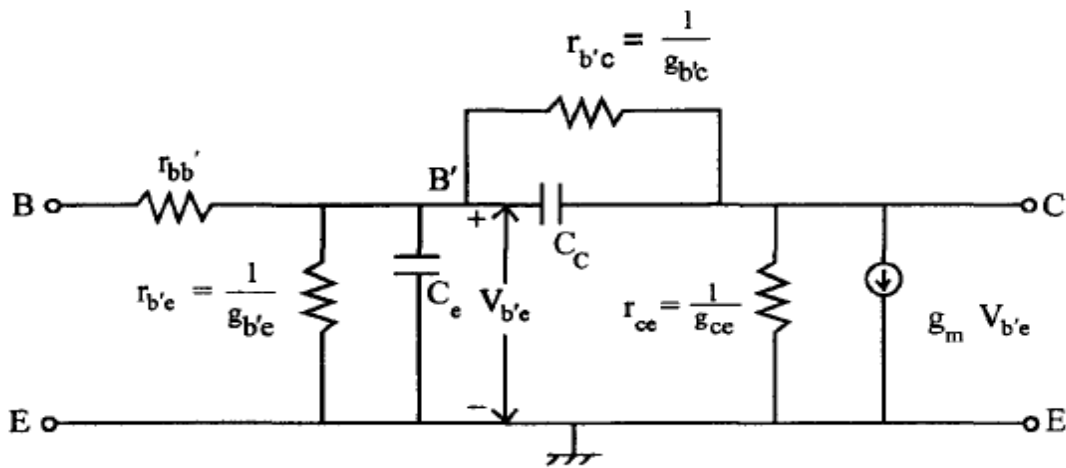


Fig. high frequency model of BJT at low frequencies

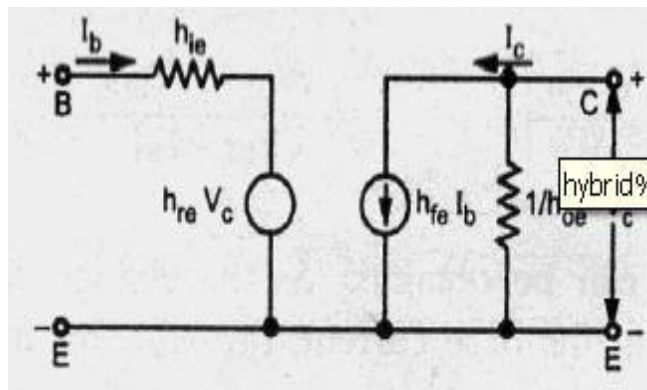


Fig hybrid model of BJT at low frequencies

The High frequency model parameters of a BJT in terms of low frequency hybrid parameters are given below:

Transconductance $g_m = I_c/V_t$

Internal Base node to emitter resistance $r_{b'e} = h_{fe}/g_m = (h_{fe} \cdot V_t)/I_c$

Internal Base node to collector resistance $r_{b'c} = (h_{re} \cdot r_{b'e}) / (1 - h_{re})$ assuming $h_{re} \ll 1$ it reduces to $r_{b'c} = (h_{re} \cdot r_{b'e})$

Base spreading resistance $r_{bb'} = h_{ie} - r_{b'e} = h_{ie} - (h_{fe} \cdot V_t)/I_c$

Collector to emitter resistance $r_{ce} = 1 / (h_{oe} - (1 + h_{fe})/r_{b'c})$

Collector Emitter Short Circuit Current Gain

Consider a single stage Common Emitter transistor amplifier circuit. The hybrid-1t equivalent circuit is as shown:

$$I_L = -g_m V_{b'e}$$

$$V_{b'e} = \frac{I_i}{g_{b'e} + j\omega(C_e + C_c)}$$

A_i under short circuit condition is,

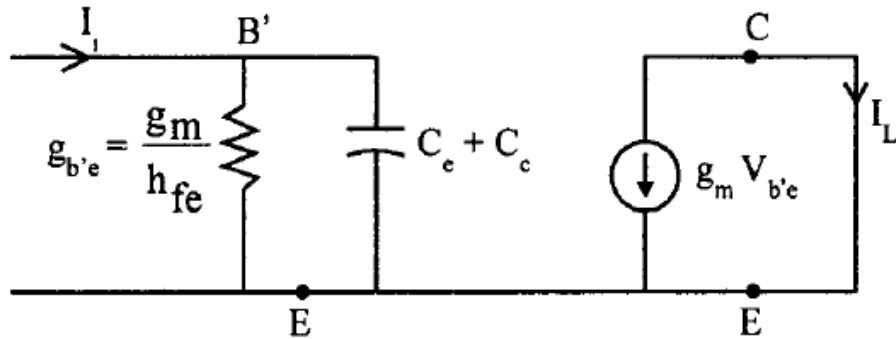
$$A_i = \frac{I_L}{I_i} = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

But $g_{b'e} = \frac{g_m}{h_{fe}}$, $C_e + C_c \simeq C_e$

$$C_e = \frac{g_m}{2\pi f_T}$$
$$= \frac{-g_m}{\frac{g_m}{h_{fe}} + j \frac{2\pi \cdot g_m \cdot f}{2\pi f_T}}$$

$\therefore A_i = \frac{-1}{\frac{1}{h_{fe}} + j \left(\frac{f}{f_T} \right)}$

If the output is shorted i.e. $R_L = 0$, what will be the flow response of this circuit? When $R_L = 0$, $V_O = 0$. Hence $A_V = 0$. So the gain that we consider here is the current gain I_L/I_i . The simplified equivalent circuit with output shorted is,



A current source gives sinusoidal current I_c . Output current or load current is I_L . $g_{b'e}$ is neglected since $g_{b'e} \ll g_m$, g_{ce} is in shunt with short circuit $R = 0$. Therefore g_{ce} disappears. The current is delivered to the output directly through C_e and $g_{b'e}$ is also neglected since this will be very small.

$$I_L = -g_m V_{b'e}$$

$$V_{b'e} = \frac{I_i}{g_{b'e} + j\omega(C_e + C_c)}$$

A_i under short circuit condition is,

$$A_i = \frac{I_L}{I_i} = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

But

$$g_{b'e} = \frac{g_m}{h_{fe}}, \quad C_e + C_c \approx C_e$$

$$C_e = \frac{g_m}{2\pi f_T}$$

$$= \frac{-g_m}{\frac{g_m}{h_{fe}} + \frac{j 2\pi \cdot g_m \cdot f}{2\pi f_T}}$$

\therefore

$$A_i = \frac{-1}{\frac{1}{h_{fe}} + j\left(\frac{f}{f_T}\right)}$$

$$= \frac{-h_{fe}}{1 + j h_{fe} \left(\frac{f}{f_T} \right)}$$

$$A_i = \frac{-h_{fe}}{1 + j \left(\frac{f}{f_\beta} \right)}$$

$$\frac{f_T}{h_{fe}} = f_\beta$$

$$|A_i| = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f}{f_\beta} \right)^2}}$$

Where $f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_c)}$

$$g_{b'e} = \frac{g_m}{h_{fe}}$$

$\therefore f_\beta = \frac{g_m}{h_{fe} 2\pi(C_e + C_c)}$

At $f = f_\beta$, $A_i = \frac{1}{\sqrt{2}} = 0.707$ of h_{fe} .

Current Gain with Resistance Load:

$$f_T = f_\beta \cdot h_{fe} = \frac{g_m}{2\pi(C_e + C_c)}$$

Considering the load resistance R_L
 $V_{b'e}$ is the input voltage and is equal to V_1
 V_{ce} is the output voltage and is equal to V_2

$$K_2 = \frac{V_{ce}}{V_{b'e}}$$

This circuit is still complicated for analysis. Because, there are two time constants associated with the input and the other associated with the output. The output time constant will be much smaller than the input time constant. So it can be neglected.

$K =$ Voltage gain. It will be $\gg 1$

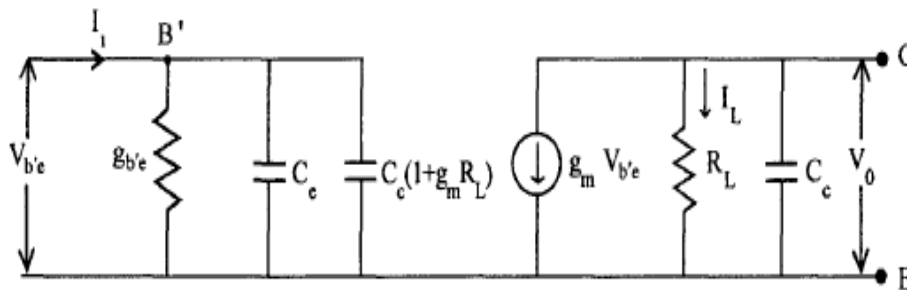
$$g_{b'e} \left(\frac{K-1}{K} \right) \simeq g_{b'e}$$

$$g_{b'e} < g_{ce} \quad \therefore \quad r_{b'e} \simeq 4 \text{ M}\Omega, \quad r_{ce} = 80 \text{ K (typical values)}$$

So $g_{b'e}$ can be neglected in the equivalent circuit. In a wide band amplifier R_L will not exceed $2\text{K}\Omega$. If R_L is small f_H is large.

$$f_H = \frac{1}{2\pi C_s (R_C \parallel R_L)}$$

Therefore g_{ce} can be neglected compared with R_L . Therefore the output circuit consists of current generator $g_m V_{b'e}$ feeding the load R_L so the Circuit simplifies as shown in Fig.



$$K = \frac{V_{ce}}{V_{b'e}} = -g_m R_L; \quad g_m = 50 \text{ mA/V}, \quad R_L = 2 \text{ k}\Omega \text{ (typical values)}$$

$$K = -100$$

Miller's Theorem

It states that if an impedance Z is connected between the input and output terminals, of a network, between which there is voltage gain, K , the same effect can be had by removing Z and connecting an impedance Z_i at the input $=Z/(1-K)$ and Z_o across the output $=ZK/(K-1)$

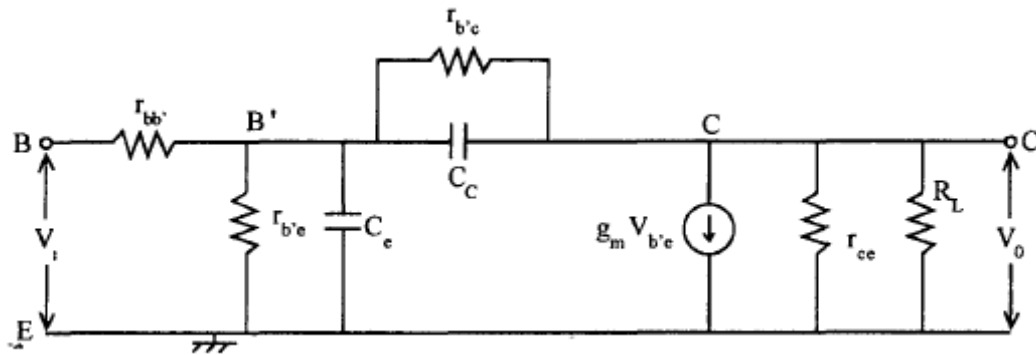


Fig. High frequency equivalent circuit with resistive load

Therefore high frequency equivalent circuit using Miller's theorem reduces

to

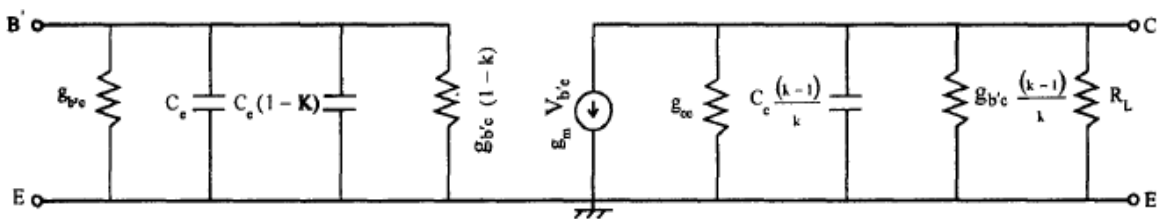


Fig. Circuit after applying Miller's Theorem

$$K = \frac{V_{ce}}{V_{b'e}}$$

$$V_{ce} = -I_c \cdot R_L$$

$$K = \frac{-I_C \cdot R_L}{V_{b'e}}$$

$$\frac{I_C}{V_{b'e}} = g_m$$

$$K = -g_m \cdot R_L$$

The Parameters f_T

f_T is the frequency at which the short circuit Common Emitter current gain becomes unity.

The Parameters f_β

$$A_i = 1, \quad \text{or} \quad \frac{h_{fe}}{\sqrt{1 + \left(\frac{f_T}{f_\beta}\right)^2}} = 1$$

$$f = f_T, \quad A_i = 1$$

$$h_{fe} = \sqrt{1 + \left(\frac{f_T}{f_\beta}\right)^2}$$

$$(h_{fe})^2 = 1 + \left(\frac{f_T}{f_\beta}\right)^2 \cong \left(\frac{f_T}{f_\beta}\right)^2$$

$$h_{fe} \cong \frac{f_T}{f_\beta} \quad \text{when } A_i = 1$$

$$\boxed{f_T \cong h_{fe} \cdot f_\beta}$$

$$f_\beta = \frac{g_m}{h_{fe} \{C_e + C_c\}}$$

$$f_T = f_\beta \cdot h_{fe} = \frac{g_m}{2\pi(C_e + C_c)}$$

$$C_e \gg C_c$$

$$\boxed{f_T \cong \frac{g_m}{2\pi C_e}}$$

$$A_i = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

Dividing by $g_{b'e}$, Numerator and Denominator,

$$A_i = \frac{-g_m |g_{b'e}}{1 + \frac{j2\pi f(C_e + C_c)}{g_{b'e}}}$$

we know that $g_{b'e} = \frac{g_m}{h_{fe}}$

$\therefore \frac{g_m}{g_{b'e}} = h_{fe}$

$$A_i = \frac{-h_{fe}}{1 + jf \left[\frac{2\pi(C_e + C_c)}{g_{b'e}} \right]}$$

But we know that $A_i = \frac{-h_{fe}}{1 + j \frac{f}{f_\beta}}$

Comparing, $f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_c)} = \frac{g_m}{h_{fe} \cdot 2\pi(C_e + C_c)} \quad \therefore g_{b'e} = \frac{g_m}{h_{fe}}$

\therefore $f_\beta = \frac{g_m}{h_{fe} \cdot 2\pi(C_e + C_c)}$

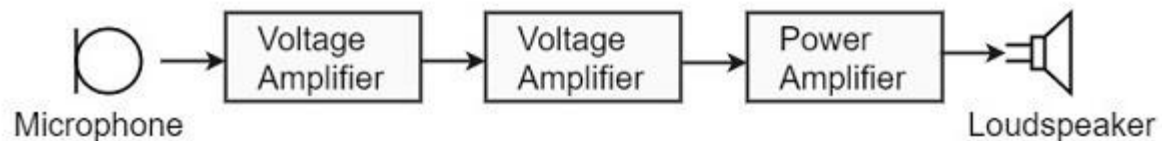
$$f_T = \frac{g_m}{2\pi(C_e + C_c)}$$

MODULE II: LARGE SIGNAL AMPLIFIERS

In practice, any amplifier consists of few stages of amplification. If we consider audio amplification, it has several stages of amplification, depending upon our requirement.

Power Amplifier

After the audio signal is converted into electrical signal, it has several voltage amplifications done, after which the power amplification of the amplified signal is done just before the loud speaker stage. This is clearly shown in the below figure.



While the voltage amplifier raises the voltage level of the signal, the power amplifier raises the power level of the signal. Besides raising the power level, it can also be said that a power amplifier is a device which converts DC power to AC power and whose action is controlled by the input signal.

The DC power is distributed according to the relation,

$$\text{DC power input} = \text{AC power output} + \text{losses}$$

Power Transistor

For such Power amplification, a normal transistor would not do. A transistor that is manufactured to suit the purpose of power amplification is called as a **Power transistor**.

A Power transistor differs from the other transistors, in the following factors.

- It is larger in size, in order to handle large powers.
- The collector region of the transistor is made large and a heat sink is placed at the collector-base junction in order to minimize heat generated.
- The emitter and base regions of a power transistor are heavily doped.
- Due to the low input resistance, it requires low input power.

Hence there is a lot of difference in voltage amplification and power amplification. So, let us now try to get into the details to understand the differences between a voltage amplifier and a power amplifier.

Difference between Voltage and Power Amplifiers

Let us try to differentiate between voltage and power amplifier.

Voltage Amplifier

The function of a voltage amplifier is to raise the voltage level of the signal. A voltage amplifier is designed to achieve maximum voltage amplification.

The voltage gain of an amplifier is given by

$$A_v = \beta(R_c/R_{in})$$

The characteristics of a voltage amplifier are as follows –

- The base of the transistor should be thin and hence the value of β should be greater than 100.
- The resistance of the input resistor R_{in} should be low when compared to collector load R_C .
- The collector load R_C should be relatively high. To permit high collector load, the voltage amplifiers are always operated at low collector current.
- The voltage amplifiers are used for small signal voltages.

Power Amplifier

The function of a power amplifier is to raise the power level of input signal. It is required to deliver a large amount of power and has to handle large current.

The characteristics of a power amplifier are as follows –

- The base of transistor is made thicken to handle large currents. The value of β being ($\beta > 100$) high.
- The size of the transistor is made larger, in order to dissipate more heat, which is produced during transistor operation.
- Transformer coupling is used for impedance matching.
- Collector resistance is made low.

The comparison between voltage and power amplifiers is given below in a tabular form.

| S.No | Particular | Voltage Amplifier | Power Amplifier |
|------|-------------------|----------------------------------|---------------------------------|
| 1 | β | High (>100) | Low (5 to 20) |
| 2 | R_C | High (4-10 K Ω) | Low (5 to 20 Ω) |
| 3 | Coupling | Usually R-C coupling | Invariably transformer coupling |
| 4 | Input voltage | Low (a few m V) | High (2-4 V) |
| 5 | Collector current | Low (≈ 1 mA) | High (> 100 mA) |
| 6 | Power output | Low | High |
| 7 | Output impedance | High (≈ 12 K Ω) | Low (200 Ω) |

The Power amplifiers amplify the power level of the signal. This amplification is done in the last stage in audio applications. The applications related to radio frequencies employ radio power amplifiers. But the **operating point** of a transistor, plays a very important role in determining the efficiency of the amplifier. The **main classification** is done based on this mode of operation.

The classification is done based on their frequencies and also based on their mode of operation.

Classification Based on Frequencies

Power amplifiers are divided into two categories, based on the frequencies they handle. They are as follows.

- **Audio Power Amplifiers** – The audio power amplifiers raise the power level of signals that have audio frequency range (20 Hz to 20 KHz). They are also known as **Small signal power amplifiers**.
- **Radio Power Amplifiers** – Radio Power Amplifiers or tuned power amplifiers raise the power level of signals that have radio frequency range (3 KHz to 300 GHz). They are also known as **large signal power amplifiers**.

Classification Based on Mode of Operation

On the basis of the mode of operation, i.e., the portion of the input cycle during which collector current flows, the power amplifiers may be classified as follows.

- **Class A Power amplifier** – When the collector current flows at all times during the full cycle of signal, the power amplifier is known as **class A power amplifier**.
- **Class B Power amplifier** – When the collector current flows only during the positive half cycle of the input signal, the power amplifier is known as **class B power amplifier**.
- **Class C Power amplifier** – When the collector current flows for less than half cycle of the input signal, the power amplifier is known as **class C power amplifier**.

There forms another amplifier called Class AB amplifier, if we combine the class A and class B amplifiers so as to utilize the advantages of both.

Before going into the details of these amplifiers, let us have a look at the important terms that have to be considered to determine the efficiency of an amplifier.

Terms Considering Performance

The primary objective of a power amplifier is to obtain maximum output power. In order to achieve this, the important factors to be considered are collector efficiency, power dissipation capability and distortion. Let us go through them in detail.

Collector Efficiency

This explains how well an amplifier converts DC power to AC power. When the DC supply is given by the battery but no AC signal input is given, the collector output at such a condition is observed as **collector efficiency**.

The collector efficiency is defined as

$$\eta = \frac{\text{average a.c. power output}}{\text{average d.c. power input to transistor}}$$

For example, if the battery supplies 15W and AC output power is 3W. Then the transistor efficiency will be 20%.

The main aim of a power amplifier is to obtain maximum collector efficiency. Hence the higher the value of collector efficiency, the efficient the amplifier will be.

Power Dissipation Capacity

Every transistor gets heated up during its operation. As a power transistor handles large currents, it gets more heated up. This heat increases the temperature of the transistor, which alters the operating point of the transistor.

So, in order to maintain the operating point stability, the temperature of the transistor has to be kept in permissible limits. For this, the heat produced has to be dissipated. Such a capacity is called as Power dissipation capability.

Power dissipation capability can be defined as the ability of a power transistor to dissipate the heat developed in it. Metal cases called heat sinks are used in order to dissipate the heat produced in power transistors.

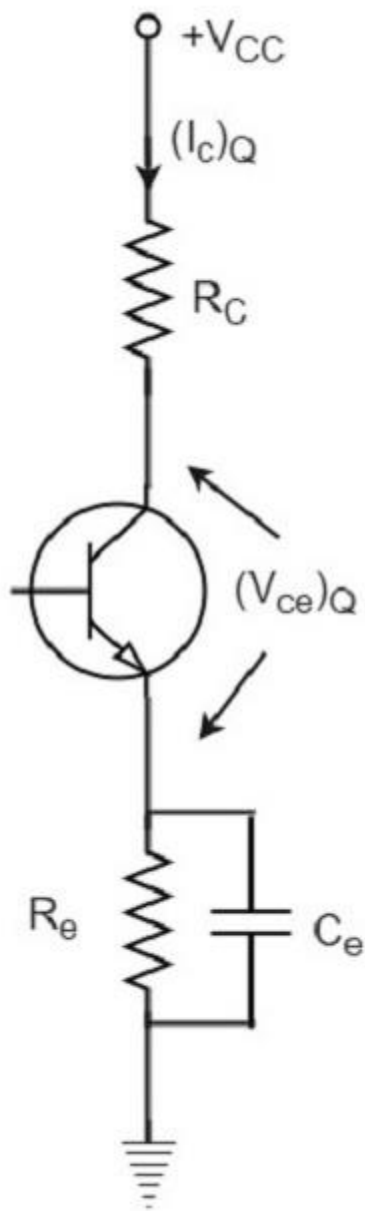
Distortion

A transistor is a non-linear device. When compared with the input, there occur few variations in the output. In voltage amplifiers, this problem is not pre-dominant as small currents are used. But in power amplifiers, as large currents are in use, the problem of distortion certainly arises.

Distortion is defined as the change of output wave shape from the input wave shape of the amplifier. An amplifier that has lesser distortion, produces a better output and hence considered efficient.

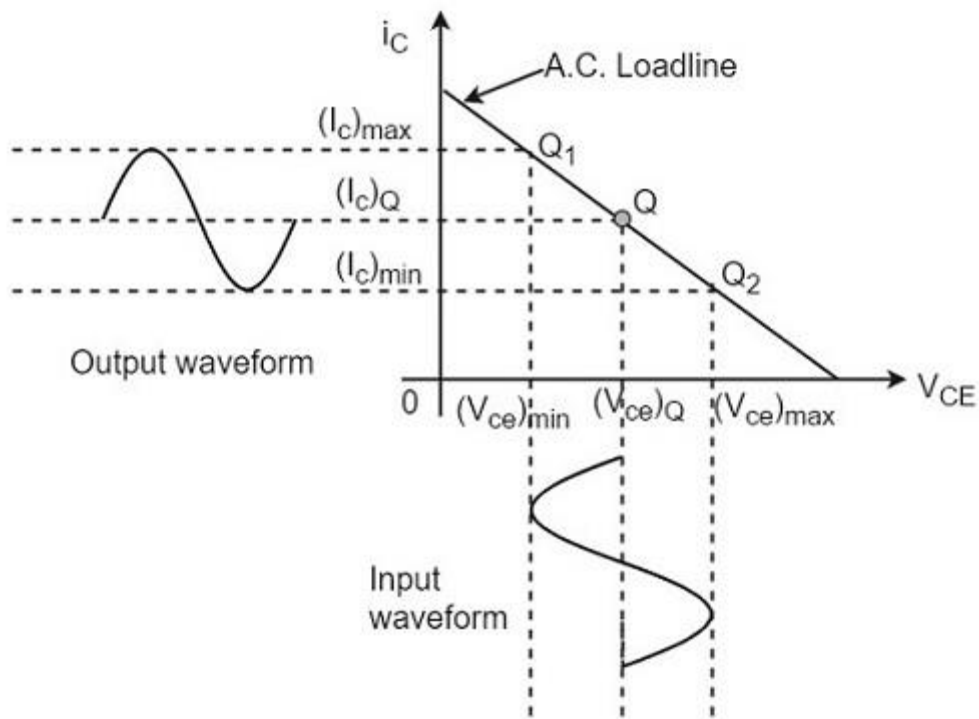
We have already come across the details of transistor biasing, which is very important for the operation of a transistor as an amplifier. Hence to achieve faithful amplification, the biasing of the transistor has to be done such that the amplifier operates over the linear region.

A Class A power amplifier is one in which the output current flows for the entire cycle of the AC input supply. Hence the complete signal present at the input is amplified at the output. The following figure shows the circuit diagram for Class A Power amplifier.



From the above figure, it can be observed that the transformer is present at the collector as a load. The use of transformer permits the impedance matching, resulting in the transference of maximum power to the load e.g. loud speaker.

The operating point of this amplifier is present in the linear region. It is so selected that the current flows for the entire ac input cycle. The below figure explains the selection of operating point.



The output characteristics with operating point Q is shown in the figure above. Here $(I_c)_Q$ and $(V_{ce})_Q$ represent no signal collector current and voltage between collector and emitter respectively. When signal is applied, the Q-point shifts to Q_1 and Q_2 . The output current increases to $(I_c)_{max}$ and decreases to $(I_c)_{min}$. Similarly, the collector-emitter voltage increases to $(V_{ce})_{max}$ and decreases to $(V_{ce})_{min}$.

D.C. Power drawn from collector battery V_{cc} is given by

$$P_{in} = \text{voltage} \times \text{current} = V_{CC}(I_C)_Q$$

This power is used in the following two parts –

- Power dissipated in the collector load as heat is given by

$$P_{RC} = (\text{current})^2 \times \text{resistance} = (I_C)^2 R_C$$

- Power given to transistor is given by

$$P_{tr} = P_{in} - P_{RC} = V_{CC} - (I_C)^2 R_C$$

When signal is applied, the power given to transistor is used in the following two parts –

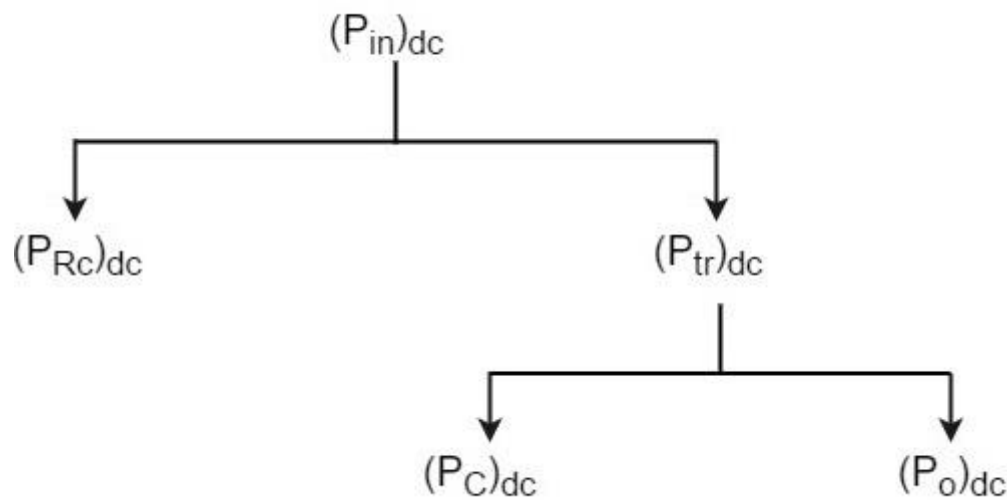
- A.C. Power developed across load resistors R_C which constitutes the a.c. power output.

$$(P_O)_{ac} = I^2 R_C = V^2 R_C = (V_m)^2 \sqrt{2}^2 R_C = V_m^2 R_C$$

Where I is the R.M.S. value of a.c. output current through load, V is the R.M.S. value of a.c. voltage, and V_m is the maximum value of V .

- The D.C. power dissipated by the transistor (collector region) in the form of heat, i.e., $(P_C)_{dc}$

We have represented the whole power flow in the following diagram.



This class A power amplifier can amplify small signals with least distortion and the output will be an exact replica of the input with increased strength.

Let us now try to draw some expressions to represent efficiencies.

Overall Efficiency

The overall efficiency of the amplifier circuit is given by

$$\begin{aligned}
 (\eta)_{\text{overall}} &= \frac{\text{a.c. power delivered to the load}}{\text{total power delivered by d.c. supply}} \\
 &= \frac{(P_O)_{\text{ac}}}{(P_{\text{in}})_{\text{dc}}}
 \end{aligned}$$

Collector Efficiency

The collector efficiency of the transistor is defined as

$$\begin{aligned}
 (\eta)_{\text{collector}} &= \frac{\text{average a.c. power output}}{\text{average d.c. power input to transistor}} \\
 &= \frac{(P_O)_{\text{ac}}}{(P_{\text{tr}})_{\text{dc}}}
 \end{aligned}$$

Expression for overall efficiency

$$\begin{aligned}
 (P_O)_{\text{ac}} &= V_{\text{rms}} \times I_{\text{rms}} \\
 &= \frac{1}{\sqrt{2}} \sqrt{[(V_{\text{ce}})_{\text{max}} - (V_{\text{ce}})_{\text{min}}]^2} \times \frac{1}{\sqrt{2}} \sqrt{[(I_{\text{C}})_{\text{max}} - (I_{\text{C}})_{\text{min}}]^2} \\
 &= \frac{1}{2} [(V_{\text{ce}})_{\text{max}} - (V_{\text{ce}})_{\text{min}}] \times [(I_{\text{C}})_{\text{max}} - (I_{\text{C}})_{\text{min}}]
 \end{aligned}$$

Therefore

$$(\eta)_{\text{overall}} = \frac{[(V_{\text{ce}})_{\text{max}} - (V_{\text{ce}})_{\text{min}}] \times [(I_{\text{C}})_{\text{max}} - (I_{\text{C}})_{\text{min}}] \times V_{\text{CC}}}{(I_{\text{C}})_{\text{Q}}}$$

Advantages of Class A Amplifiers

The advantages of Class A power amplifier are as follows –

- The current flows for complete input cycle
- It can amplify small signals

- The output is same as input
- No distortion is present

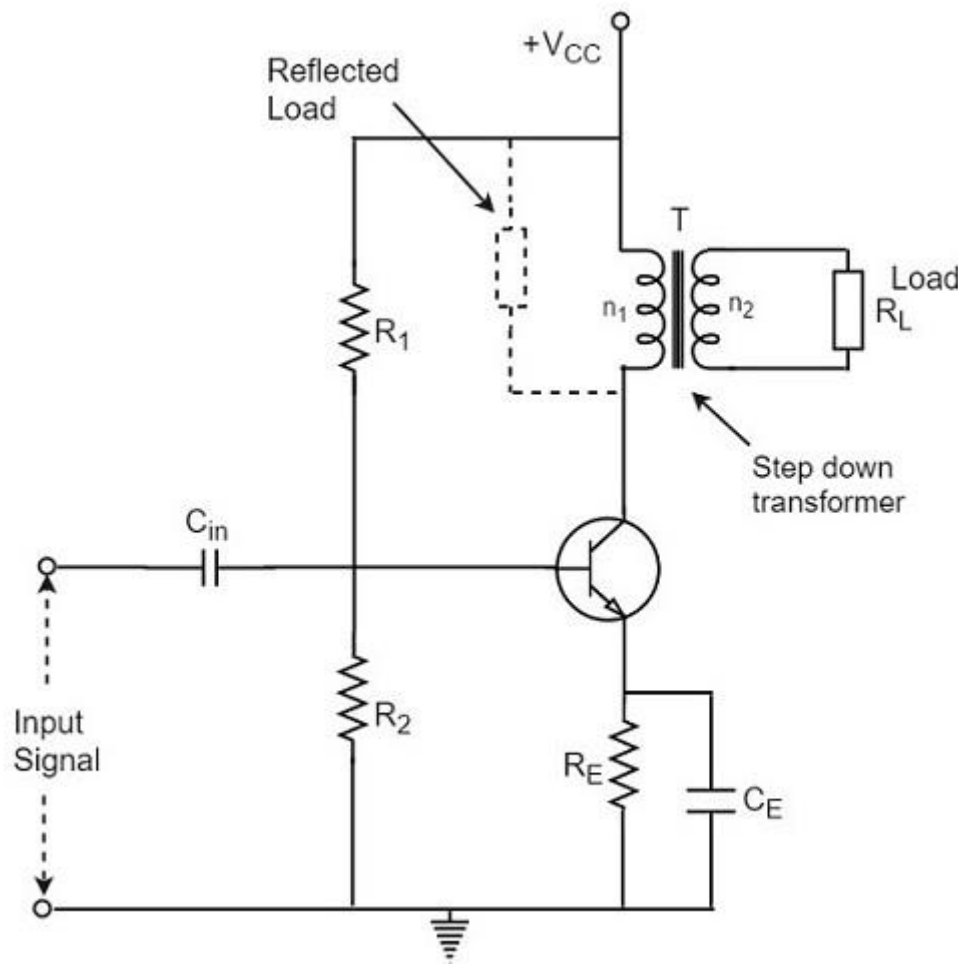
Disadvantages of Class A Amplifiers

The advantages of Class A power amplifier are as follows –

- Low power output
- Low collector efficiency.

The class A power amplifier as discussed in the previous chapter, is the circuit in which the output current flows for the entire cycle of the AC input supply. We also have learnt about the disadvantages it has such as low output power and efficiency. In order to minimize those effects, the transformer coupled class A power amplifier has been introduced.

The **construction of class A power amplifier** can be understood with the help of below figure. This is similar to the normal amplifier circuit but connected with a transformer in the collector load.



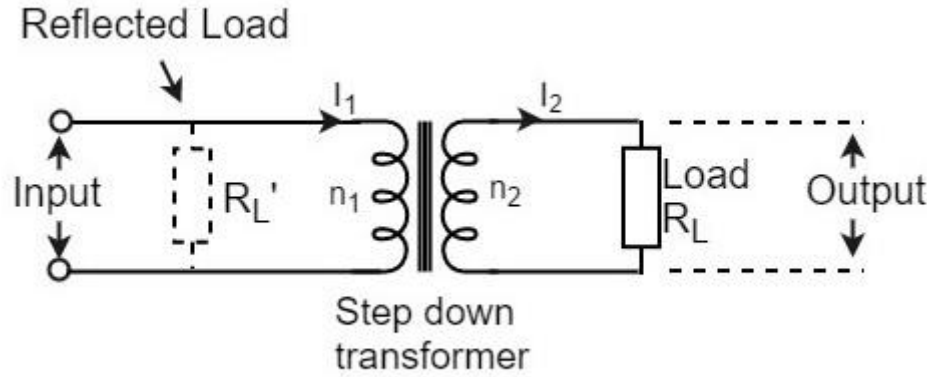
Here R_1 and R_2 provide potential divider arrangement. The resistor R_e provides stabilization, C_e is the bypass capacitor and R_e to prevent a.c. voltage. The transformer used here is a step-down transformer.

The high impedance primary of the transformer is connected to the high impedance collector circuit. The low impedance secondary is connected to the load (generally loud speaker).

Transformer Action

The transformer used in the collector circuit is for impedance matching. R_L is the load connected in the secondary of a transformer. R_L' is the reflected load in the primary of the transformer.

The number of turns in the primary are n_1 and the secondary are n_2 . Let V_1 and V_2 be the primary and secondary voltages and I_1 and I_2 be the primary and secondary currents respectively. The below figure shows the transformer clearly.



We know that

$$V_1 V_2 = n_1 n_2 \text{ and } I_1 I_2 = n_1 n_2$$

Or

$$V_1 = n_1 n_2 V_2 \text{ and } I_1 = n_1 n_2 I_2$$

Hence

$$V_1 I_1 = (n_1 n_2)^2 V_2 I_2$$

But $V_1 / I_1 = R_L' = \text{effective input resistance}$

And $V_2 / I_2 = R_L = \text{effective output resistance}$

Therefore,

$$R_L' = (n_1 n_2)^2 R_L = n^2 R_L$$

Where

$$n = \frac{\text{number of turns in primary}}{\text{number of turns in secondary}} = \frac{n_1}{n_2}$$

A power amplifier may be matched by taking proper turn ratio in step down transformer.

Circuit Operation

If the peak value of the collector current due to signal is equal to zero signal collector current, then the maximum a.c. power output is obtained. So, in order to achieve complete amplification, the operating point should lie at the center of the load line.

The operating point obviously varies when the signal is applied. The collector voltage varies in opposite phase to the collector current. The variation of collector voltage appears across the primary of the transformer.

Circuit Analysis

The power loss in the primary is assumed to be negligible, as its resistance is very small.

The input power under dc condition will be

$$(P_{in})_{dc} = (P_{tr})_{dc} = V_{CC} \times (I_C)_{Q}$$

Under maximum capacity of class A amplifier, voltage swings from $(V_{ce})_{max}$ to zero and current from $(I_c)_{max}$ to zero.

Hence

$$V_{rms} = \frac{1}{\sqrt{2}} \sqrt{(V_{ce})_{max} - (V_{ce})_{min}} = \frac{1}{\sqrt{2}} \sqrt{(V_{ce})_{max}} = \frac{V_{CC}}{2\sqrt{2}} = \frac{V_{CC}}{2\sqrt{2}}$$

$$I_{rms} = \frac{1}{\sqrt{2}} \sqrt{(I_c)_{max} - (I_c)_{min}} = \frac{1}{\sqrt{2}} \sqrt{(I_c)_{max}} = \frac{(I_c)_{Q2}}{2\sqrt{2}} = \frac{(I_c)_{Q2}}{2\sqrt{2}}$$

Therefore,

$$(P_{O})_{ac} = V_{rms} \times I_{rms} = \frac{V_{CC}}{2\sqrt{2}} \times \frac{(I_c)_{Q2}}{2\sqrt{2}} = \frac{V_{CC} \times (I_c)_{Q2}}{4}$$

Therefore,

$$\text{Collector Efficiency} = \frac{(P_{O})_{ac}}{(P_{T})_{dc}} = \frac{(P_{O})_{ac}}{(P_{T})_{dc}}$$

Or,

$$\begin{aligned} (\eta)_{\text{collector}} &= \frac{V_{CC} \times (I_c)_{Q2} \times V_{CC} \times (I_c)_{Q2}}{12 \times V_{CC} \times (I_c)_{Q2}} = 12 \times \frac{V_{CC} \times (I_c)_{Q2} \times V_{CC} \times (I_c)_{Q2}}{12 \times V_{CC} \times (I_c)_{Q2}} \\ &= 12 \times 100 = 50\% = 12 \times 100 = 50\% \end{aligned}$$

The efficiency of a class A power amplifier is nearly than 30% whereas it has got improved to 50% by using the transformer coupled class A power amplifier.

Advantages

The advantages of transformer coupled class A power amplifier are as follows.

- No loss of signal power in the base or collector resistors.
- Excellent impedance matching is achieved.
- Gain is high.
- DC isolation is provided.

Disadvantages

The disadvantages of transformer coupled class A power amplifier are as follows.

- Low frequency signals are less amplified comparatively.
- Hum noise is introduced by transformers.
- Transformers are bulky and costly.
- Poor frequency response.

Applications

The applications of transformer coupled class A power amplifier are as follows.

- This circuit is where impedance matching is the main criterion.
- These are used as driver amplifiers and sometimes as output amplifiers.

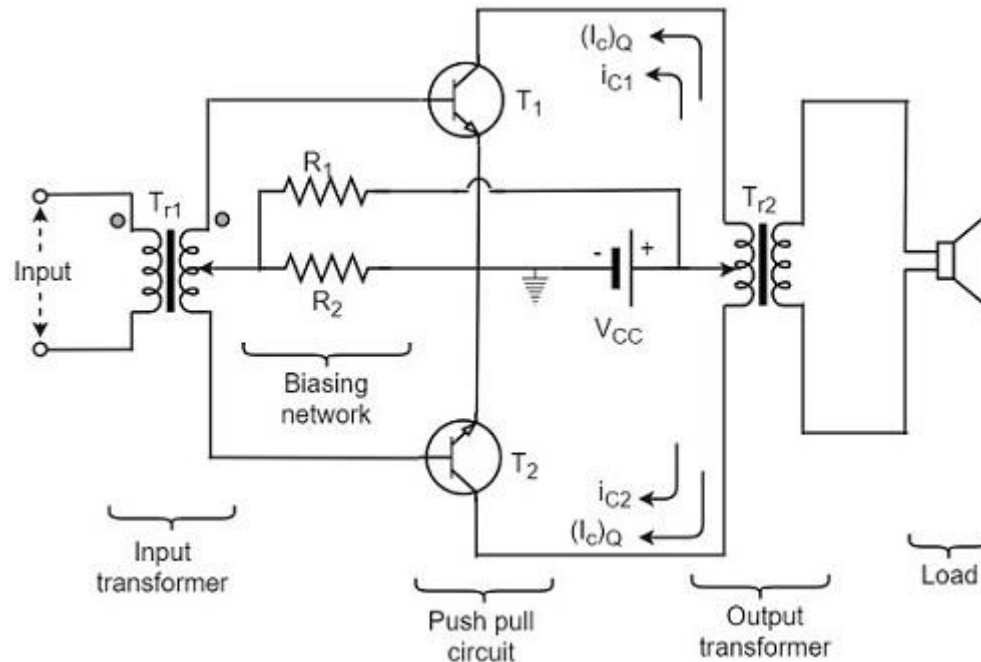
The main problems that should be dealt with are low power output and efficiency. It is possible to obtain greater power output and efficiency than that of the Class A amplifier by using a combinational transistor pair called as **Push-Pull** configuration.

In this circuit, we use two complementary transistors in the output stage with one transistor being an NPN or N-channel type while the other transistor is a PNP or P-channel (the complement) type

connected in order to operate them like **PUSH a transistor to ON** and **PULL another transistor to OFF** at the same time. This push-pull configuration can be made in class A, class B, class C or class AB amplifiers.

Construction of Push-Pull Class A Power Amplifier

The construction of the class A power amplifier circuit in push-pull configuration is shown as in the figure below. This arrangement mainly reduces the harmonic distortion introduced by the non-linearity of the transfer characteristics of a single transistor amplifier.



In Push-pull arrangement, the two identical transistors T_1 and T_2 have their emitter terminals shorted. The input signal is applied to the transistors through the transformer T_{r1} which provides opposite polarity signals to both the transistor bases. The collectors of both the transistors are connected to the primary of output transformer T_{r2} . Both the transformers are center tapped. The V_{CC} supply is provided to the collectors of both the transistors through the primary of the output transformer.

The resistors R_1 and R_2 provide the biasing arrangement. The load is generally a loudspeaker which is connected across the secondary of the output transformer. The turns ratio of the output transformer is chosen in such a way that the load is well matched with the output impedance of the transistor. So maximum power is delivered to the load by the amplifier.

Circuit Operation

The output is collected from the output transformer T_{r2} . The primary of this transformer T_{r2} has practically no dc component through it. The transistors T_1 and T_2 have their collectors connected to the primary of transformer T_{r2} so that their currents are equal in magnitude and flow in opposite directions through the primary of transformer T_{r2} .

When the a.c. input signal is applied, the base of transistor T_1 is more positive while the base of transistor T_2 is less positive. Hence the collector current i_{c1} of transistor T_1 increases while the collector current i_{c2} of transistor T_2 decreases. These currents flow in opposite directions in two halves of the primary of output transformer. Moreover, the flux produced by these currents will also be in opposite directions.

Hence, the voltage across the load will be induced voltage whose magnitude will be proportional to the difference of collector currents i.e.

$$(i_{c1} - i_{c2})(i_{c1} - i_{c2})$$

Similarly, for the negative input signal, the collector current i_{c2} will be more than i_{c1} . In this case, the voltage developed across the load will again be due to the difference

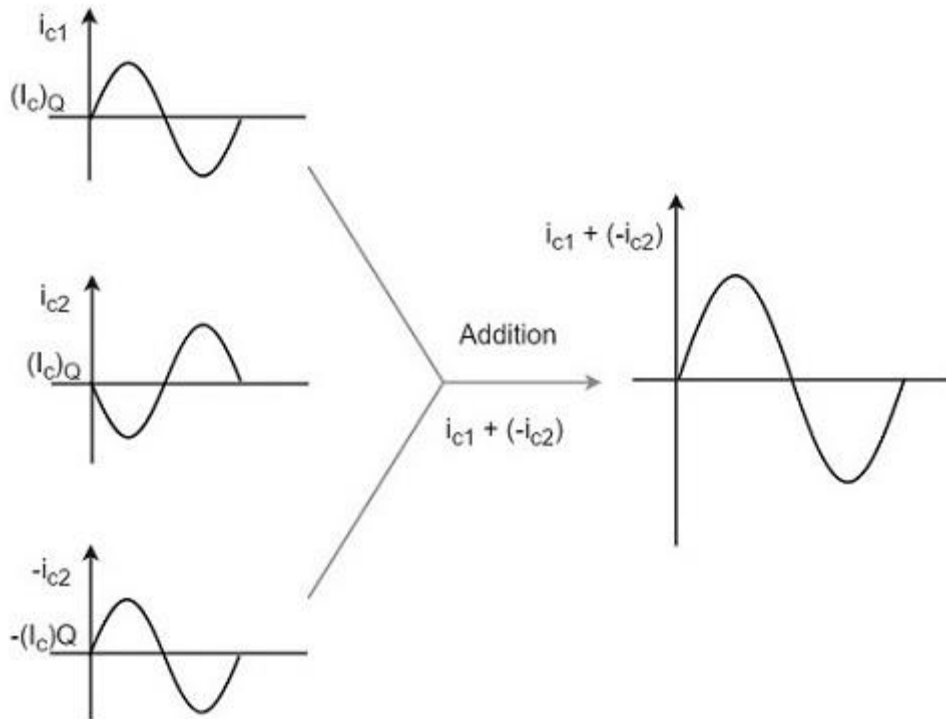
$$(i_{c1}-i_{c2})(i_{c1}-i_{c2})$$

$$\text{As } i_{c2} > i_{c1} \quad i_{c2} > i_{c1}$$

The polarity of voltage induced across load will be reversed.

$$i_{c1}-i_{c2}=i_{c1}+(-i_{c2}) \quad i_{c1}-i_{c2}=i_{c1}+(-i_{c2})$$

To have a better understanding, let us consider the below figure.



The overall operation results in an a.c. voltage induced in the secondary of output transformer and hence a.c. power is delivered to that load.

It is understood that, during any given half cycle of input signal, one transistor is being driven (or pushed) deep into conduction while the other being non-conducting (pulled out). Hence the name **Push-pull amplifier**. The harmonic distortion in Push-pull amplifier is minimized such that all the even harmonics are eliminated.

Advantages

The advantages of class A Push-pull amplifier are as follows

- High a.c. output is obtained.
- The output is free from even harmonics.
- The effect of ripple voltages are balanced out. These are present in the power supply due to inadequate filtering.

Disadvantages

The disadvantages of class A Push-pull amplifier are as follows

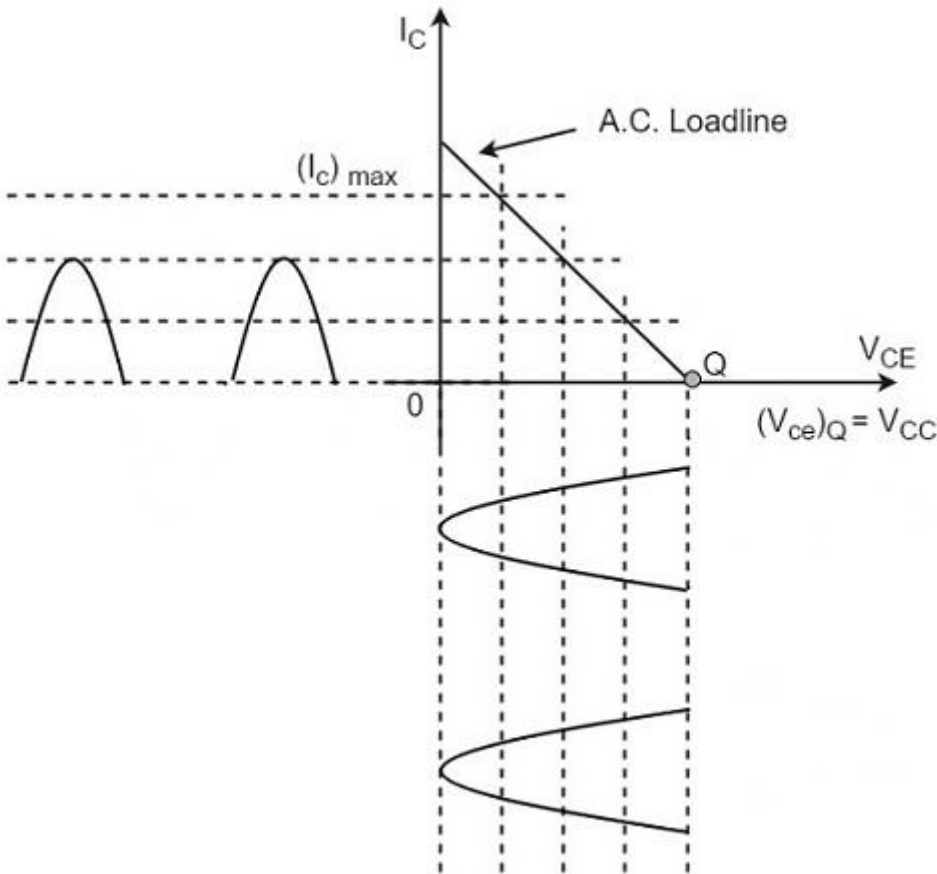
- The transistors are to be identical, to produce equal amplification.
- Center-tapping is required for the transformers.
- The transformers are bulky and costly.

When the collector current flows only during the positive half cycle of the input signal, the power amplifier is known as **class B power amplifier**.

Class B Operation

The biasing of the transistor in class B operation is in such a way that at zero signal condition, there will be no collector current. The **operating point** is selected to be at collector cut off voltage. So, when the signal is applied, **only the positive half cycle** is amplified at the output.

The figure below shows the input and output waveforms during class B operation.



When the signal is applied, the circuit is forward biased for the positive half cycle of the input and hence the collector current flows. But during the negative half cycle of the input, the circuit is reverse biased and the collector current will be absent. Hence **only the positive half cycle** is amplified at the output.

As the negative half cycle is completely absent, the signal distortion will be high. Also, when the applied signal increases, the power dissipation will be more. But when compared to class A power amplifier, the output efficiency is increased.

Well, in order to minimize the disadvantages and achieve low distortion, high efficiency and high output power, the push-pull configuration is used in this class B amplifier.

Class B Push-Pull Amplifier

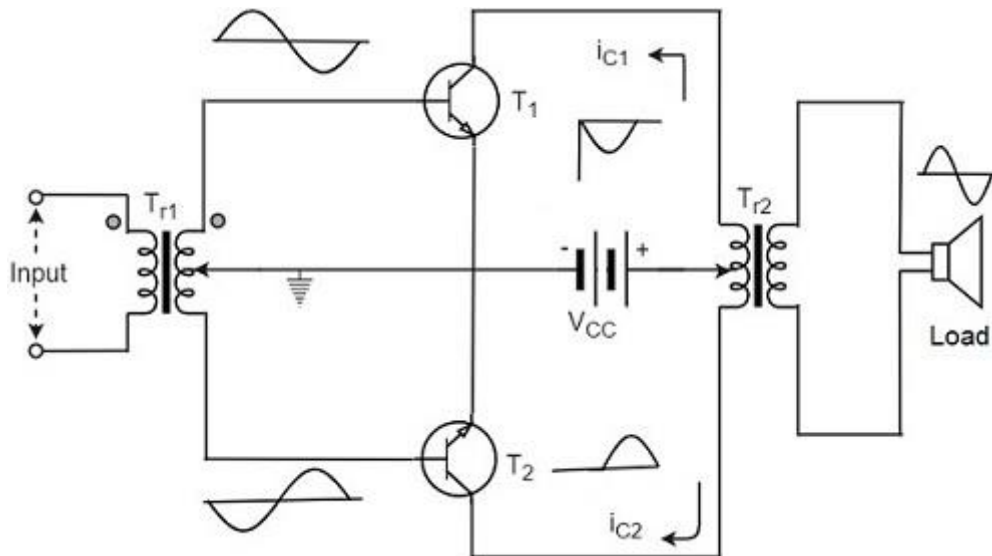
Though the efficiency of class B power amplifier is higher than class A, as only one half cycle of the input is used, the distortion is high. Also, the input power is not completely utilized. In order to compensate these problems, the push-pull configuration is introduced in class B amplifier.

Construction

The circuit of a push-pull class B power amplifier consists of two identical transistors T_1 and T_2 whose bases are connected to the secondary of the center-tapped input transformer T_{r1} . The

emitters are shorted and the collectors are given the V_{CC} supply through the primary of the output transformer T_{r2} .

The circuit arrangement of class B push-pull amplifier, is same as that of class A push-pull amplifier except that the transistors are biased at cut off, instead of using the biasing resistors. The figure below gives the detailing of the construction of a push-pull class B power amplifier.

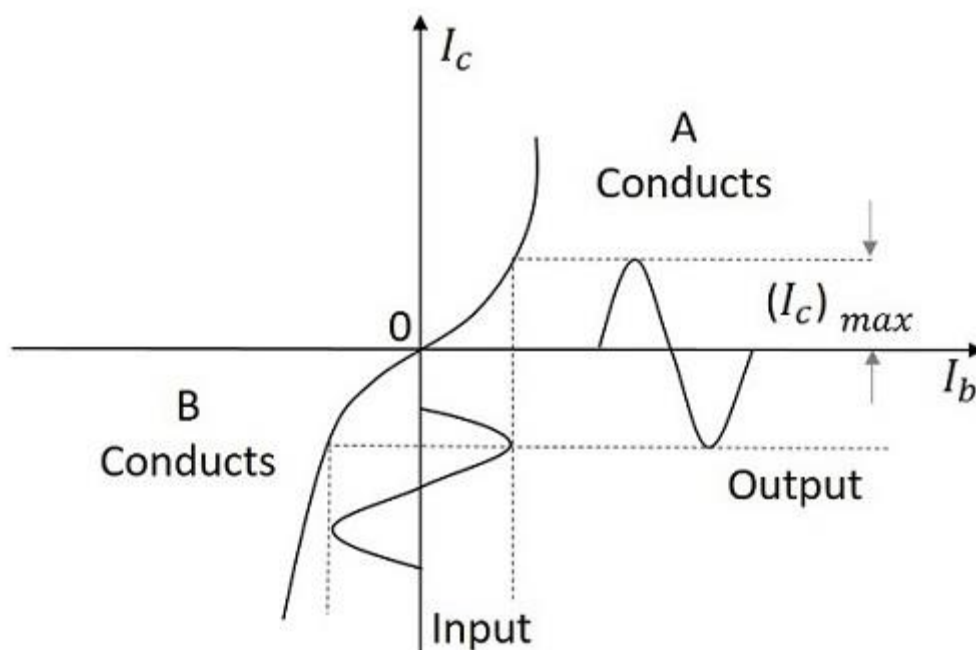


The circuit operation of class B push pull amplifier is detailed below.

Operation

The circuit of class B push-pull amplifier shown in the above figure clears that both the transformers are center-tapped. When no signal is applied at the input, the transistors T_1 and T_2 are in cut off condition and hence no collector currents flow. As no current is drawn from V_{CC} , no power is wasted.

When input signal is given, it is applied to the input transformer T_{r1} which splits the signal into two signals that are 180° out of phase with each other. These two signals are given to the two identical transistors T_1 and T_2 . For the positive half cycle, the base of the transistor T_1 becomes positive and collector current flows. At the same time, the transistor T_2 has negative half cycle, which throws the transistor T_2 into cutoff condition and hence no collector current flows. The waveform is produced as shown in the following figure.



For the next half cycle, the transistor T_1 gets into cut off condition and the transistor T_2 gets into conduction, to contribute the output. Hence for both the cycles, each transistor conducts alternately. The output transformer T_{r3} serves to join the two currents producing an almost undistorted output waveform.

Power Efficiency of Class B Push-Pull Amplifier

The current in each transistor is the average value of half sine loop.

For half sine loop, I_{dc} is given by

$$I_{dc} = (I_C)_{max} \pi \quad I_{dc} = (I_C)_{max} \pi$$

Therefore,

$$(P_{in})_{dc} = 2 \times [(I_C)_{max} \pi \times V_{CC}] \quad (P_{in})_{dc} = 2 \times [(I_C)_{max} \pi \times V_{CC}]$$

Here factor 2 is introduced as there are two transistors in push-pull amplifier.

R.M.S. value of collector current = $(I_C)_{max} / 2 - \sqrt{(I_C)_{max} / 2}$

R.M.S. value of output voltage = $V_{CC} / 2 - \sqrt{V_{CC} / 2}$

Under ideal conditions of maximum power

Therefore,

$$(P_{O})_{ac} = (I_C)_{max} 2 - \sqrt{\times V_{CC} 2 - \sqrt{}} = (I_C)_{max} \times V_{CC} 2 \quad (P_{O})_{ac} = (I_C)_{max} 2 \times V_{CC} 2 = (I_C)_{max} \times V_{CC} 2$$

Now overall maximum efficiency

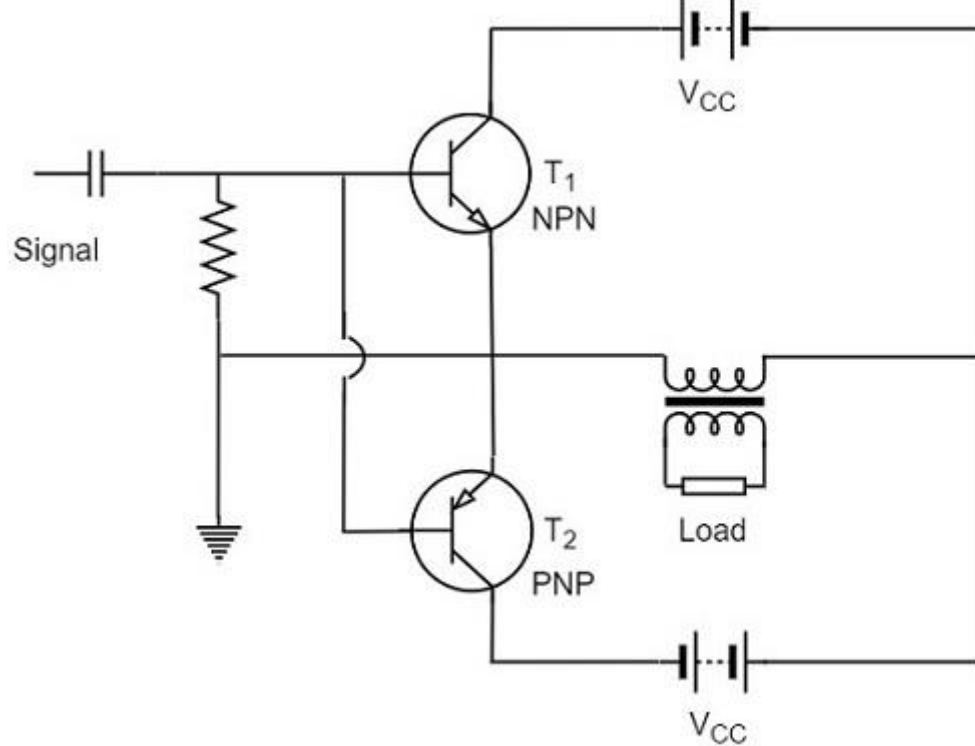
$$\begin{aligned} \eta_{overall} &= (P_{O})_{ac} / (P_{in})_{dc} \quad \eta_{overall} = (P_{O})_{ac} / (P_{in})_{dc} \\ &= (I_C)_{max} \times V_{CC} 2 \times \pi 2 / (I_C)_{max} \times V_{CC} = (I_C)_{max} \times V_{CC} 2 \times \pi 2 / (I_C)_{max} \times V_{CC} \\ &= \pi 4 = 0.785 = 78.5\% \quad = \pi 4 = 0.785 = 78.5\% \end{aligned}$$

The collector efficiency would be the same.

Hence the class B push-pull amplifier improves the efficiency than the class A push-pull amplifier.

Complementary Symmetry Push-Pull Class B Amplifier

The push pull amplifier which was just discussed improves efficiency but the usage of center-tapped transformers makes the circuit bulky, heavy and costly. To make the circuit simple and to improve the efficiency, the transistors used can be complemented, as shown in the following circuit diagram.



The above circuit employs a NPN transistor and a PNP transistor connected in push pull configuration. When the input signal is applied, during the positive half cycle of the input signal, the NPN transistor conducts and the PNP transistor cuts off. During the negative half cycle, the NPN transistor cuts off and the PNP transistor conducts.

In this way, the NPN transistor amplifies during positive half cycle of the input, while PNP transistor amplifies during negative half cycle of the input. As the transistors are both complementary to each other, yet act symmetrically while being connected in push pull configuration of class B, this circuit is termed as **Complementary symmetry push pull class B amplifier**.

Advantages

The advantages of Complementary symmetry push pull class B amplifier are as follows.

- As there is no need of center tapped transformers, the weight and cost are reduced.
- Equal and opposite input signal voltages are not required.

Disadvantages

The disadvantages of Complementary symmetry push pull class B amplifier are as follows.

- It is difficult to get a pair of transistors (NPN and PNP) that have similar characteristics.
- We require both positive and negative supply voltages.

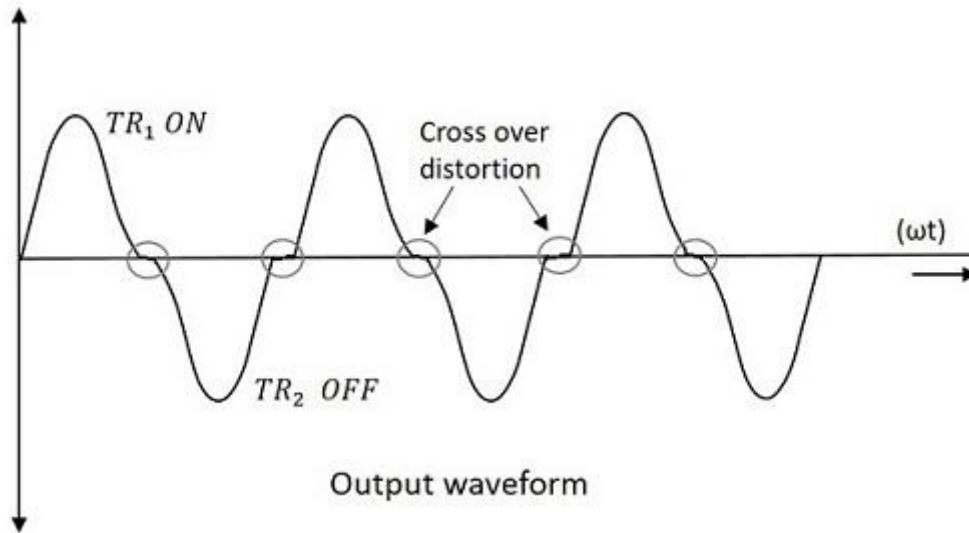
The class A and class B amplifier so far discussed has got few limitations. Let us now try to combine these two to get a new circuit which would have all the advantages of both class A and class B amplifier without their inefficiencies. Before that, let us also go through another important problem, called as **Cross over distortion**, the output of class B encounters with.

Cross-over Distortion

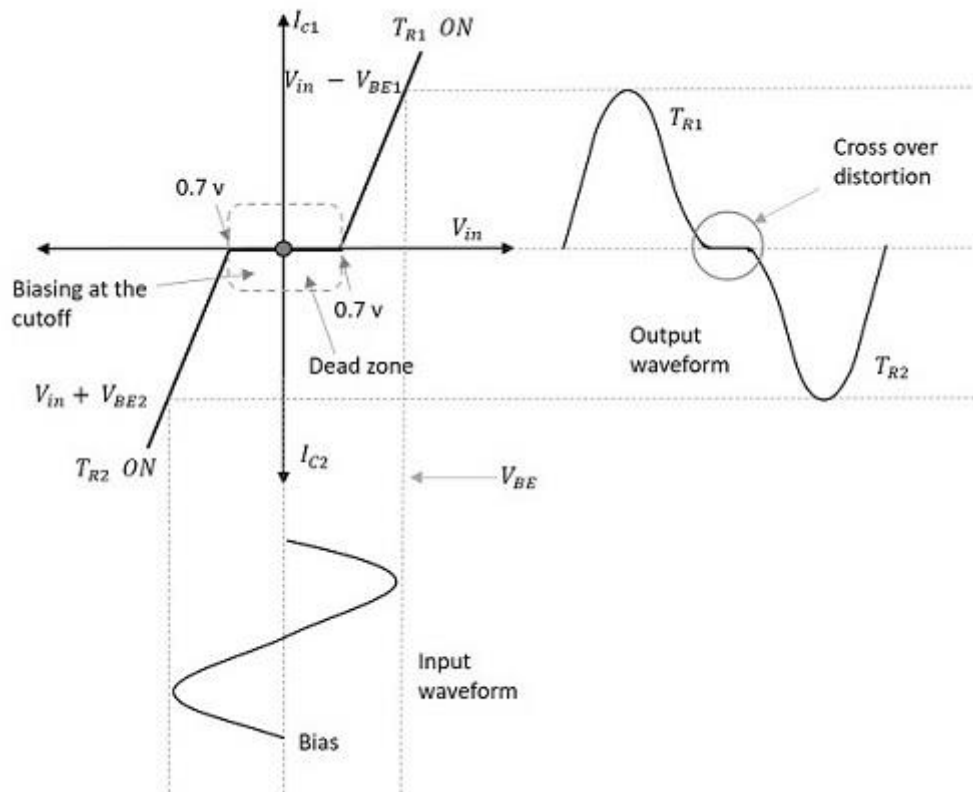
In the push-pull configuration, the two identical transistors get into conduction, one after the other and the output produced will be the combination of both.

When the signal changes or crosses over from one transistor to the other at the zero voltage point, it produces an amount of distortion to the output wave shape. For a transistor in order to conduct, the base emitter junction should cross 0.7v, the cut off voltage. The time taken for a transistor to get ON from OFF or to get OFF from ON state is called the **transition period**.

At the zero voltage point, the transition period of switching over the transistors from one to the other, has its effect which leads to the instances where both the transistors are OFF at a time. Such instances can be called as **Flat spot** or **Dead band** on the output wave shape.



The above figure clearly shows the cross over distortion which is prominent in the output waveform. This is the main disadvantage. This cross over distortion effect also reduces the overall peak to peak value of the output waveform which in turn reduces the maximum power output. This can be more clearly understood through the non-linear characteristic of the waveform as shown below.



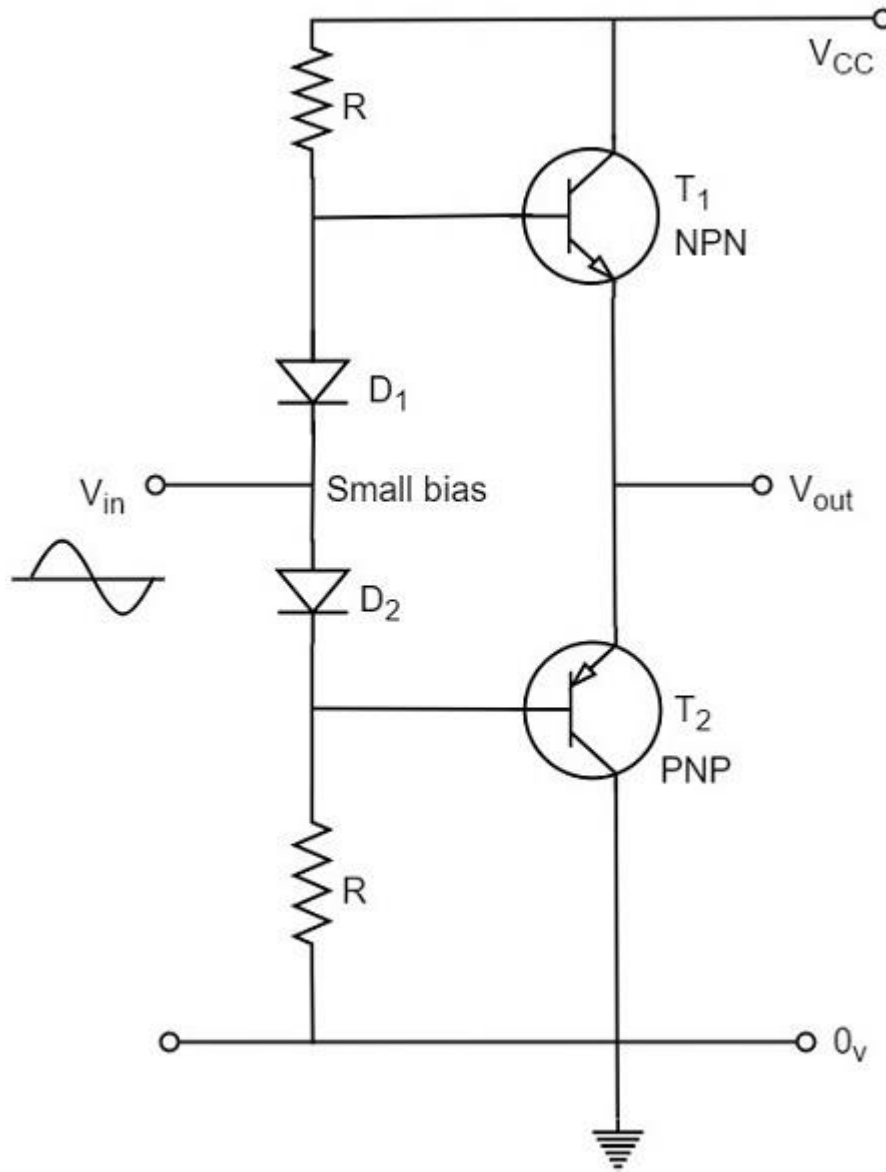
It is understood that this cross-over distortion is less pronounced for large input signals, where as it causes severe disturbance for small input signals. This cross over distortion can be eliminated if the conduction of the amplifier is more than one half cycle, so that both the transistors won't be OFF at the same time.

This idea leads to the invention of class AB amplifier, which is the combination of both class A and class B amplifiers, as discussed below.

Class AB Power Amplifier

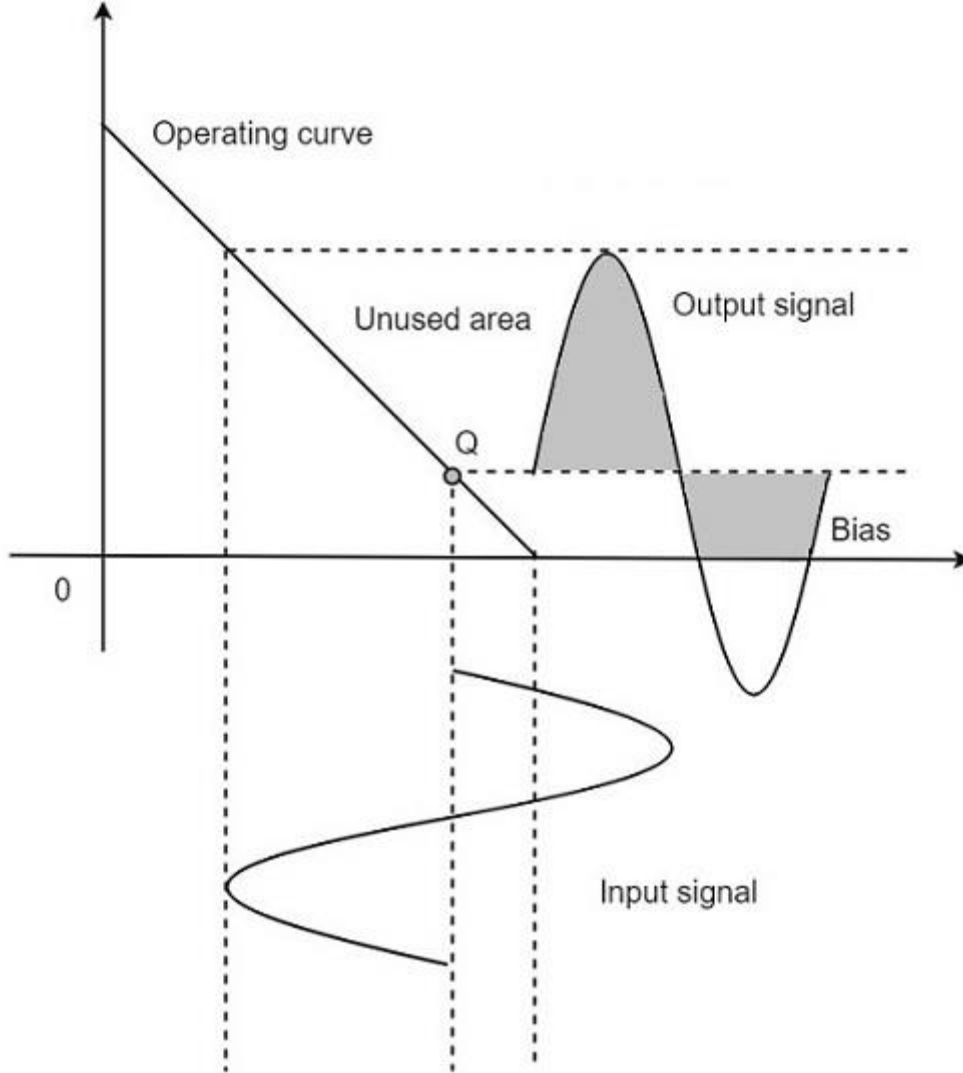
As the name implies, class AB is a combination of class A and class B type of amplifiers. As class A has the problem of low efficiency and class B has distortion problem, this class AB is emerged to eliminate these two problems, by utilizing the advantages of both the classes.

The cross over distortion is the problem that occurs when both the transistors are OFF at the same instant, during the transition period. In order to eliminate this, the condition has to be chosen for more than one half cycle. Hence, the other transistor gets into conduction, before the operating transistor switches to cut off state. This is achieved only by using class AB configuration, as shown in the following circuit diagram.



Therefore, in class AB amplifier design, each of the push-pull transistors is conducting for slightly more than the half cycle of conduction in class B, but much less than the full cycle of conduction of class A.

The conduction angle of class AB amplifier is somewhere between 180° to 360° depending upon the operating point selected. This is understood with the help of below figure.

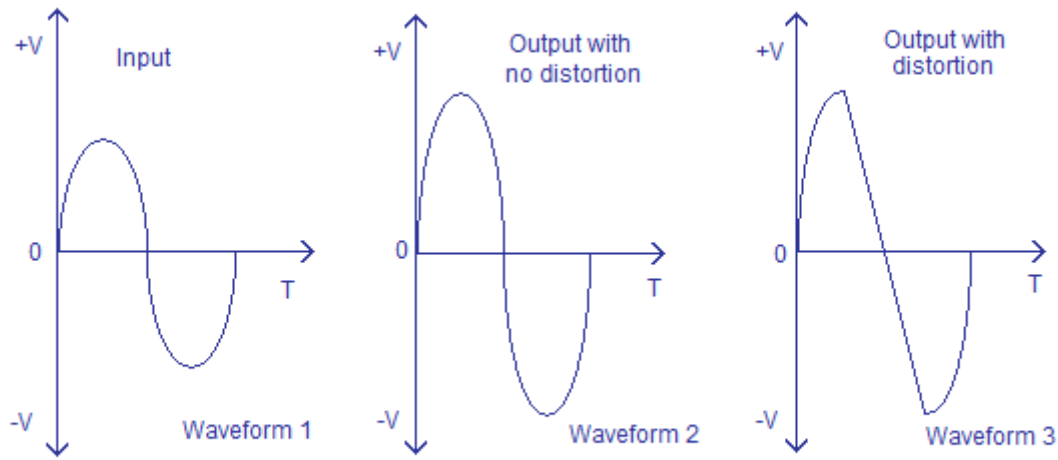


The small bias voltage given using diodes D_1 and D_2 , as shown in the above figure, helps the operating point to be above the cutoff point. Hence the output waveform of class AB results as seen in the above figure. The crossover distortion created by class B is overcome by this class AB, as well the inefficiencies of class A and B don't affect the circuit.

So, the class AB is a good compromise between class A and class B in terms of efficiency and linearity having the efficiency reaching about 50% to 60%. The class A, B and AB amplifiers are called as **linear amplifiers** because the output signal amplitude and phase are linearly related to the input signal amplitude and phase.

Harmonic distortion in power amplifiers.

Distortion is a serious problem faced in power amplifier design. In faithful amplification the output signal must be a scaled replica of the input signal and if there is any dissimilarity between the input and output waveform, then the output is said to be distorted. Unpleasant sound output coming from an audio system, which is no more the faithful reproduction of the original audio is mainly due to distortion. Other reasons for bad sound output are noise, clipping etc and they are not discussed here. The figure given below shows faithful amplification and distorted amplification.



Distortion in power amplifiers

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In the above figure you can see that every point in the input waveform (waveform1) is exactly reproduced in the non distorted output (waveform2) and the falling edges of the input waveform are unfaithfully reproduced in the distorted output (waveform 3).

Harmonic distortion.

Harmonic distortion can be explained as any distortion or corruption in the output waveform due to the generation of harmonics. The integer multiples of a fundamental frequency are called harmonics. In audio amplifier domain, the frequency of the input signal is taken as the fundamental frequency. For example, if “x” is the fundamental frequency then 1x,2x, 3x, 4x.....nx are the harmonics.

Harmonic distortion in power amplifiers are mainly caused by the non linearities of the active elements (transistors). The active element used for amplification whether BJT, FET, MOSFET or anything like that may not equally amplify every points in the input waveform and this is the reason behind the non-linearity. In different amplifier configurations Class A has the highest linearity, then class AB, then Class B and finally Class C has the worst linearity.

How well designed the audio amplifier may be , its output might contain some distortion mainly in the form of even harmonics. Out of the even harmonics 2nd order harmonics will be generally the prominent one. Second order harmonic distortion is the amount of 2nd order harmonic content present in the output signal with respect to the fundamental frequency.

MODULE III: LINEAR WAVE SHAPING

A linear network is a network made up of linear elements only. A linear network can be described by linear differential equations. The principle of superposition and the principle of homogeneity hold good for linear networks. In pulse circuitry, there are a number of waveforms, which appear very frequently. The most important of these are sinusoidal, step, pulse, square wave, ramp, and exponential waveforms. The response of RC , RL , and RLC circuits to these signals is described in this chapter. Out of these signals, the sinusoidal signal has a unique characteristic that it preserves its shape when it is transmitted through a linear network, i.e. under steady state, the output will be a precise reproduction of the input sinusoidal signal. There will only be a change in the amplitude of the signal and there may be a phase shift between the input and the output waveforms. The influence of the circuit on the signal may then be completely specified by the ratio of the output to the input amplitude and by the phase angle between the output and the input. No other periodic waveform preserves its shape precisely when transmitted through a linear network, and in many cases the output signal may bear very little resemblance to the input signal.

The process whereby the form of a non-sinusoidal signal is altered by transmission through a linear network is called linear wave shaping.

THE HIGH-PASS RC CIRCUIT

Figure 1.30 shows a high-pass RC circuit. At zero frequency the reactance of the capacitor is infinity and so it blocks the input and hence the output is zero. Hence, this capacitor is called the *blocking capacitor* and this circuit, also called the *capacitive coupling circuit*, is used to provide dc isolation between the input and the output. As the frequency increases, the reactance of the capacitor decreases and hence the output and gain increase. At very high frequencies, the capacitive reactance is very small so a very small voltage appears, across C and, so the output is almost equal to the input and the gain is equal to 1. Since this circuit attenuates low-frequency signals and allows transmission of high-frequency signals with little or no attenuation, it is called a high-pass circuit.

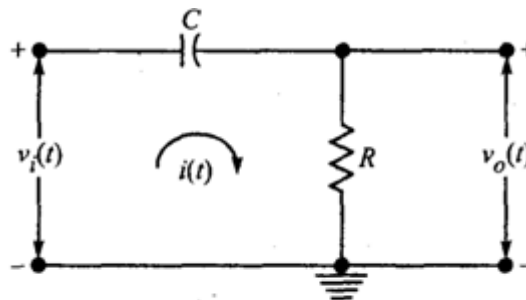


Figure The high-pass RC circuit.

Sinusoidal Input

Figure (a) shows the Laplace transformed high-pass RC circuit. The gain versus frequency curve of a high-pass circuit excited by a sinusoidal input is shown in Figure (b). For a sinusoidal input v_i , the output signal v_o increases in amplitude with increasing frequency. The frequency at which the gain is $1/\sqrt{2}$ of its maximum value is called the lower cut-off or lower 3-dB frequency. For a high-pass circuit, there is no upper cut-off frequency because all high frequency signals are transmitted with zero attenuation. Therefore, $f_2 - f_1$. Hence bandwidth $B.W = f_2 - f_1 = \infty$

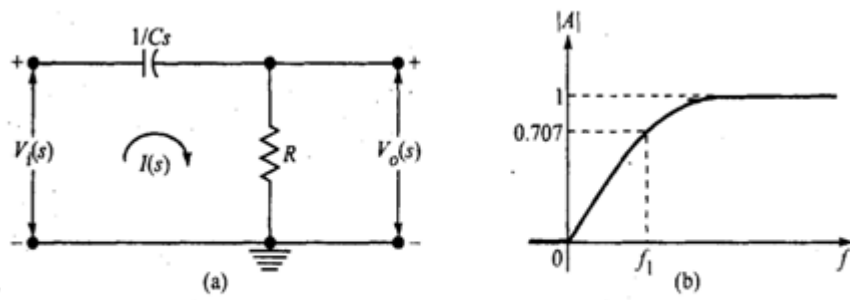


Figure (a) Laplace transformed high-pass circuit and (b) gain versus frequency plot.

Expression for the lower cut-off frequency

For the high-pass RC circuit shown in Figure (a), the magnitude of the steady-state gain A , and the angle θ by which the output leads the input are given by

$$A = \frac{V_o(s)}{V_i(s)} = \frac{R}{R + \frac{1}{Cs}} = \frac{1}{1 + \frac{1}{RCs}}$$

Putting

$$s = j\omega; \quad A = \frac{1}{1 - j\frac{1}{\omega RC}} = \frac{1}{1 - j\frac{1}{2\pi f RC}}$$

$$\therefore |A| = \frac{1}{\sqrt{1 + \left(\frac{1}{2\pi f RC}\right)^2}} \quad \text{and} \quad \theta = -\tan^{-1} \frac{1}{2\pi f RC}$$

At the lower cut-off frequency f_1 , $|A| = 1/\sqrt{2}$

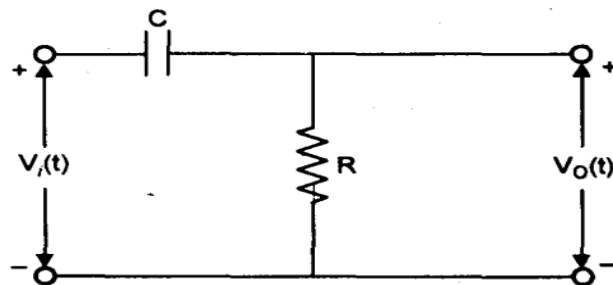
$$\therefore \frac{1}{\sqrt{1 + \left(\frac{1}{2\pi f_1 RC}\right)^2}} = \frac{1}{\sqrt{2}}$$

Squaring and equating the denominators,

$$\frac{1}{2\pi f_1 RC} = 1 \quad \text{i.e.} \quad f_1 = \frac{1}{2\pi RC}$$

This is the expression for the lower cut-off frequency of a high-pass circuit.

High pass RC circuit response to Step input Voltage:



RC high-pass filter

A step waveform is defined by the following expression:

$$v(t) = \begin{cases} 0 & \text{for } t < 0 \\ V & \text{for } t \geq 0 \end{cases}$$

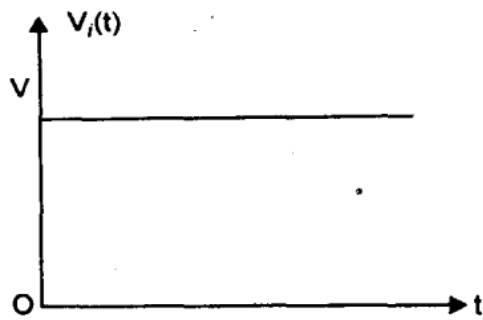


Fig:a The step waveform

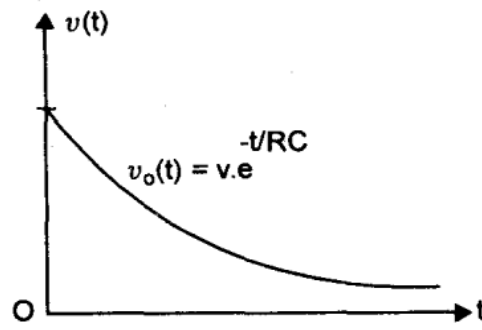


Fig:b Output waveform

The generalized transient expression has been derived at,

$$v_o(t) = v_o(\infty) + [v_o(0) - v_o(\infty)]e^{-t/RC} \quad \text{--- (1)}$$

The expression for $v(t)$ can be found if we know the initial condition $v(0)$ final condition $v(\infty)$, and the time constant 'RC' of the circuit.

$$\begin{aligned} v_o(t) &= 0 + (V - 0)e^{-t/RC} \\ v_o(t) &= V.e^{-t/RC} \end{aligned} \quad \text{--- (2)}$$

The output waveform for the step input to an RC high pass filter is an exponentially falling waveform as shown in Fig. (b). This response reaches almost zero after a time 't' greater than '5RC'.

High pass RC circuit response to pulse input:

A positive pulse is mathematically represented as the combination of a positive step followed by a delayed negative step i.e., $v_i = Vu(t) - Vu(t - tp)$ where, tp is the duration of the pulse as shown in Fig.

To understand the response of a high-pass circuit to this pulse input, let us trace the sequence of events following the application of the input signal.

At $t = 0$, v_i abruptly rises to V . As a capacitor is connected between the input and output, the output also changes abruptly by the same amount. As the input remains constant, the output decays exponentially to V_1 at $t = tp$. Therefore,

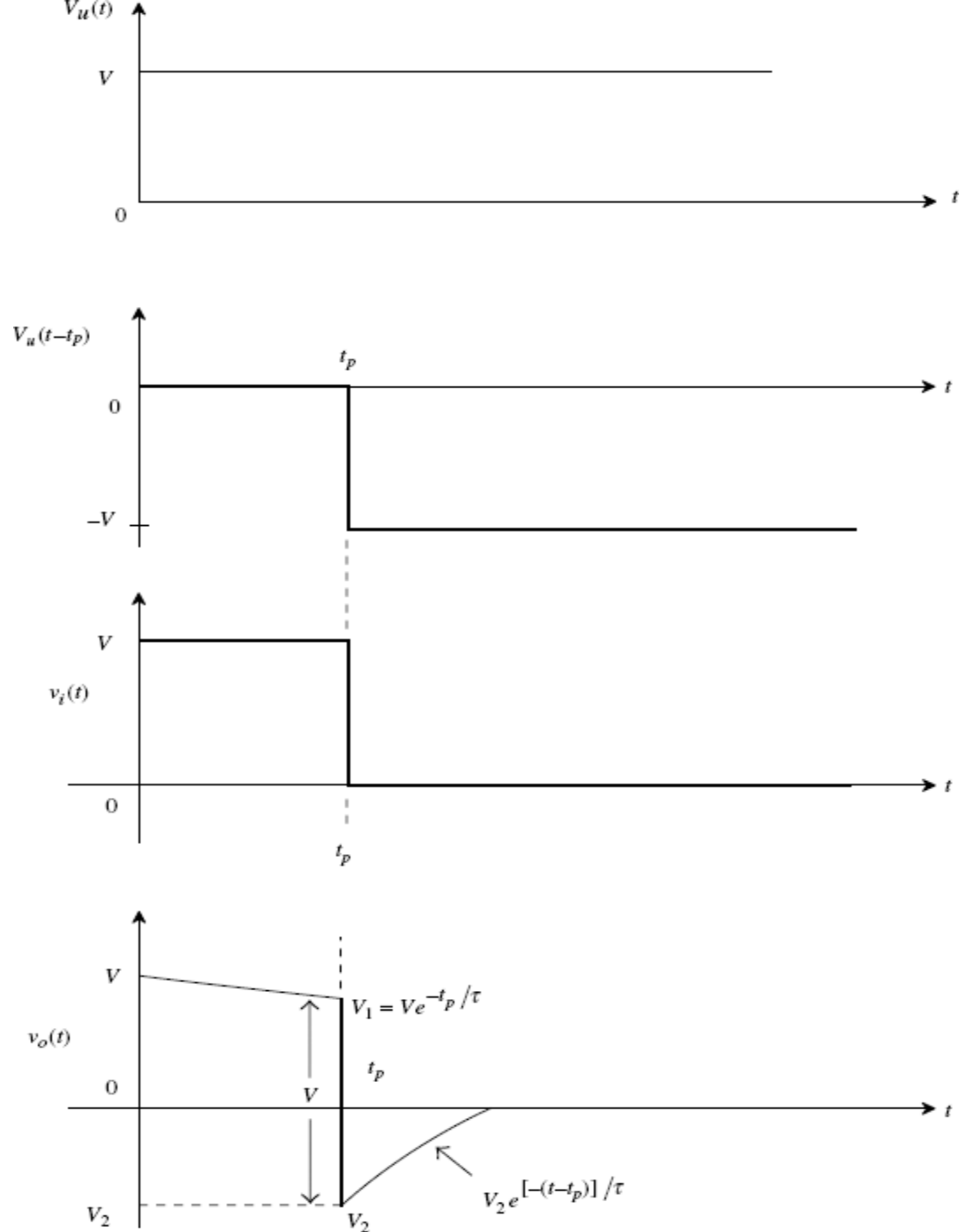
$$V_1 = Ve^{-tp/\tau}$$

At $t = tp$, the input abruptly falls by V , v_o also falls by the same amount. In other words, $v_o = V_1 - V$. Since V_1 is less than V ; v_o is negative and its value is V_2 and this decays to zero exponentially. For $t > tp$,

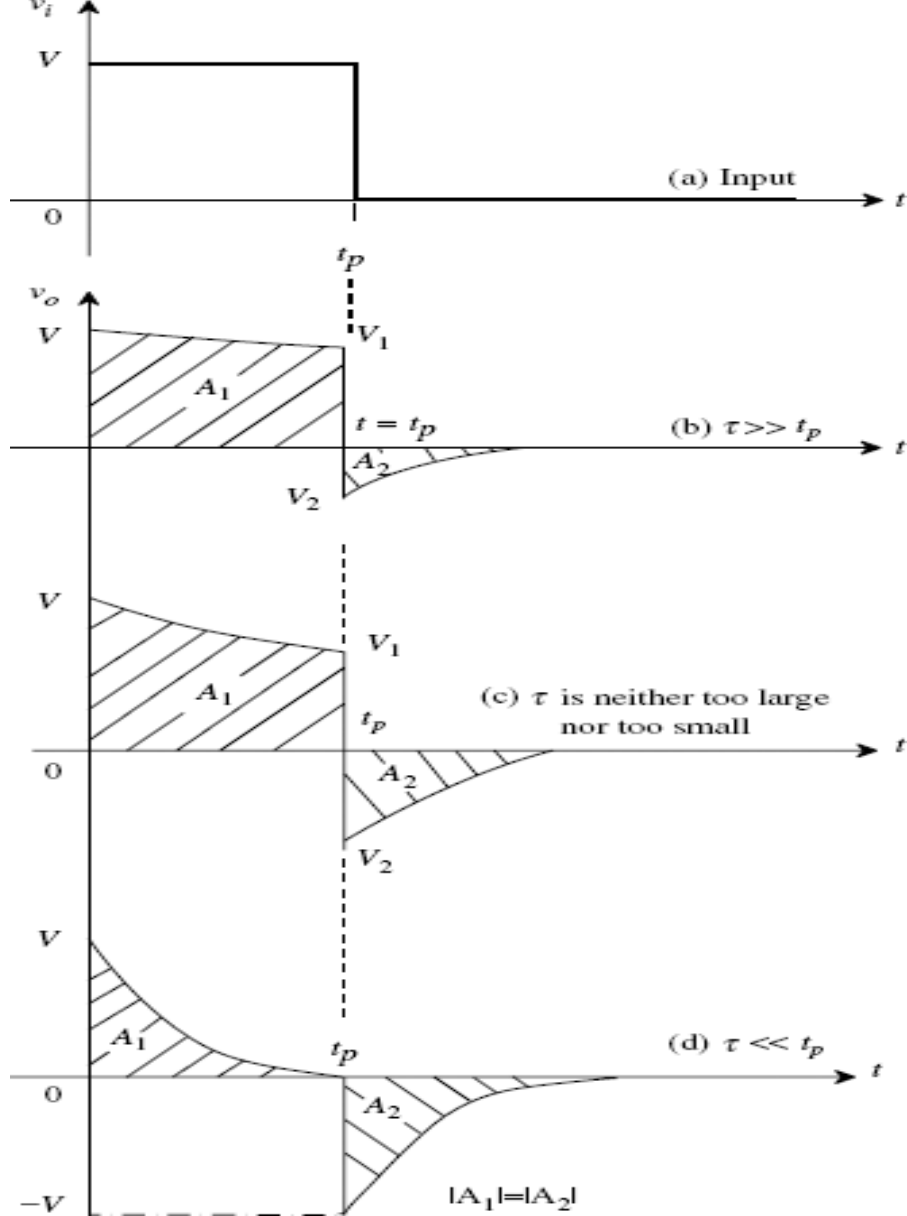
$$v_o = V_2 e^{[-(t-tp)]/\tau} = (V_1 - V) e^{[-(t-tp)]/\tau}$$

then

$$v_o = V(e^{-tp/\tau} - 1) e^{[-(t-tp)]/\tau}$$



The response of high-pass circuits with different values of τ to pulse input is plotted in Fig below. As is evident from the preceding discussion, when a pulse is passed through a high-pass circuit, it gets distorted. Only when the time constant τ is very large, the shape of the pulse at the output is preserved, as can be seen from Fig (b). However, as shown in Fig (c), when the time constant τ is neither too small nor too large, there is a tilt (also called a sag) at the top of the pulse and an under-shoot at the end of the pulse. If $\tau \ll t_p$, as in Fig (d), the output comprises a positive spike at the beginning of the pulse and a negative spike at the end of the pulse. In other words, a high-pass circuit converts a pulse into spikes by employing a small time constant; this process is called peaking.



If the distortion is to be negligible, τ has to be significantly larger than the duration of the pulse. In general, there is an undershoot at the end of the pulse. The larger the tilt (for small τ), the larger the undershoot and the smaller the time taken for this undershoot to decay to zero. The area above the reference level (A_1) is the same as the area below the reference level (A_2). Let us verify this using below Fig

Area A_1 : For $0 < t < t_p$:

$$v_o = Ve^{-t/\tau}$$

$$A_1 = \int_0^{t_p} Ve^{-t/\tau} dt = [-V\tau e^{-t/\tau}]_0^{t_p}$$

$$A_1 = [-V\tau e^{-t_p/\tau} + V\tau] = V\tau(1 - e^{-t_p/\tau})$$

Similarly,

$$A_2 = \int_{t_p}^{\infty} V(e^{-t_p/\tau} - 1)e^{-(t-t_p)/\tau} dt = \int_{t_p}^{\infty} [Ve^{-t/\tau} - Ve^{-(t-t_p)/\tau}] dt$$

$$= \left[\frac{Ve^{-t/\tau}}{-1/\tau} \right]_{t_p}^{\infty} - \left[V \frac{1}{-1/\tau} e^{-(t-t_p)/\tau} \right]_{t_p}^{\infty}$$

$$A_2 = [V\tau e^{-t_p/\tau} - V\tau] = -V\tau(1 - e^{-t_p/\tau})$$

So that,

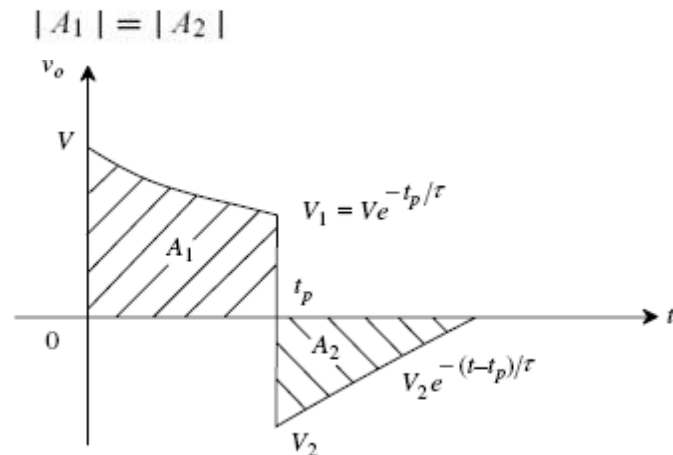


Fig: The calculation of A1 and A2

High pass RC circuit response to Square input:

A waveform that has constant amplitude, say, V' for a time T_1 and has another constant amplitude, V'' for a time T_2 , and which is repetitive with a time $T = (T_1 + T_2)$, is called a square wave. In a symmetric square wave, $T_1 = T_2 = T/2$. Figure 1.10 shows typical input-output waveforms of the high-pass circuit when a square wave is applied as the input signal.

As the capacitor blocks the DC, the DC component in the output is zero. Thus, as expected, even if the signal at the input is referenced to an arbitrary dc level, the output is always referenced to the zero level. It can be proved that whatever the dc component associated with a periodic input waveform, the dc level of the steady-state output signal for the high-pass circuit is always zero as shown in Fig. 1.10. To verify this statement, we write the KVL equation for the high-pass circuit:

$$v_i = \frac{q}{c} + v_o$$

where, q is the charge on the capacitor. Differentiating with respect to t :

$$\frac{dv_i}{dt} = \frac{1}{C} \frac{dq}{dt} + \frac{dv_o}{dt}$$

But $i = \frac{dq}{dt}$

Substituting this condition in above Eq, then

$$\frac{dv_i}{dt} = \frac{i}{C} + \frac{dv_o}{dt}$$

Since $v_o = iR$, $i = v_o/R$ and $RC = \tau$. Therefore,

$$\therefore \frac{dv_i}{dt} = \frac{v_o}{\tau} + \frac{dv_o}{dt}$$

Multiplying by dt and integrating over the time period T we get:

$$\int_0^T dv_i = [v_i]_0^T = v_i(T) - v_i(0)$$

$$\int_0^T \frac{v_o}{\tau} dt = \frac{1}{\tau} \int_0^T v_o dt$$

$$\int_0^T dv_o = [v_o]_0^T = v_o(T) - v_o(0)$$

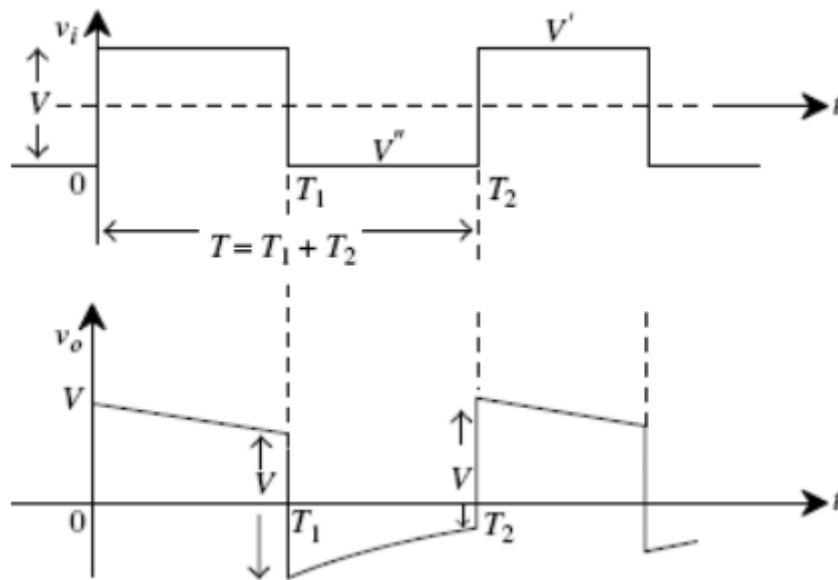


Fig: A typical steady - state output of a high - pass circuit with a square wave as input

$$v_i(T) - v_i(0) = \frac{1}{\tau} \int_0^T v_o dt + [v_o(T) - v_o(0)]$$

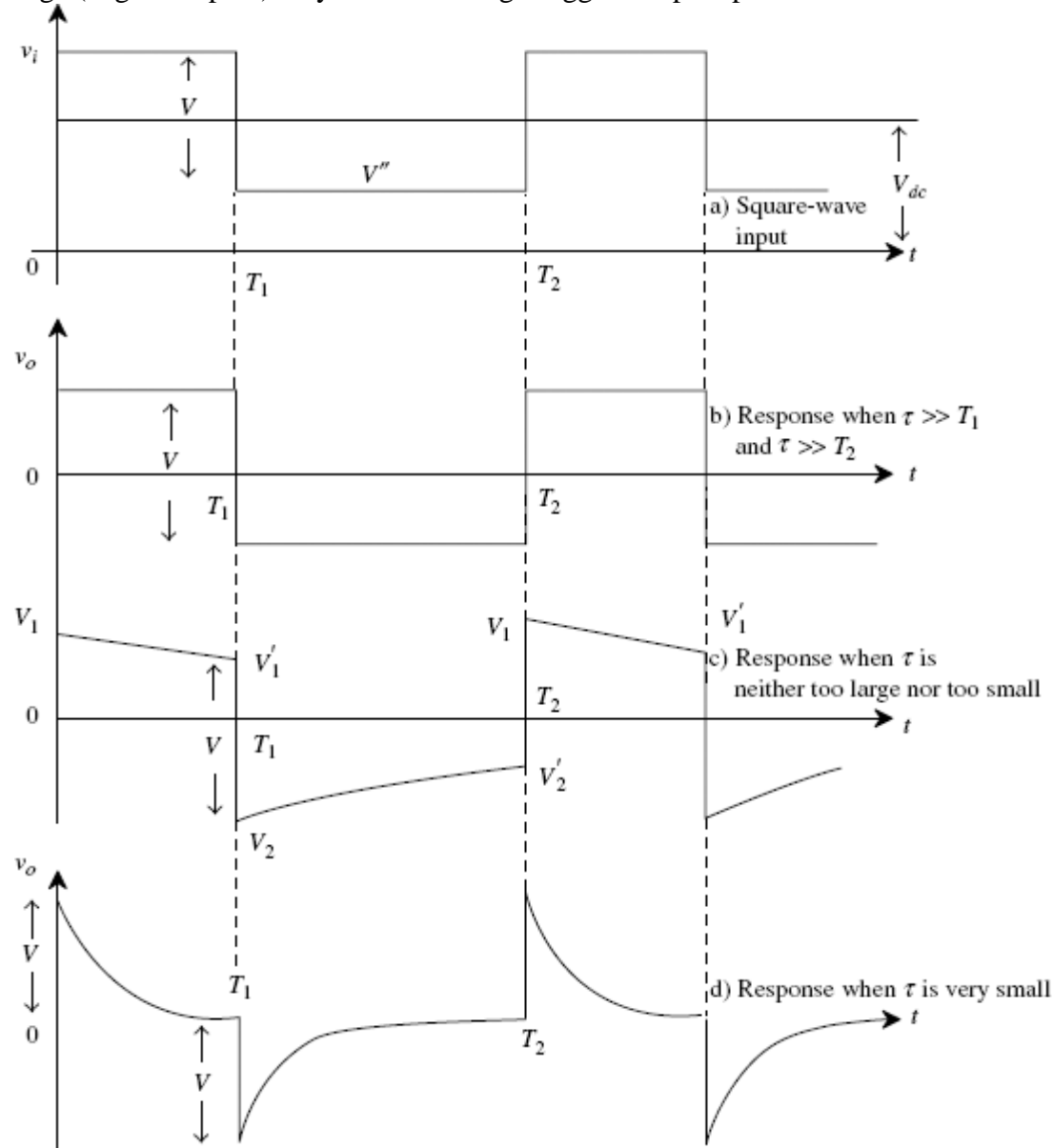
Under steady state conditions, the output and the input waveforms are repetitive with a time Period T . Therefore, $v_i(T) = v_o(T)$ and $v_i(0) = v_o(0)$. Hence, from the above Eq.

$$\int_0^T v_o dt = 0$$

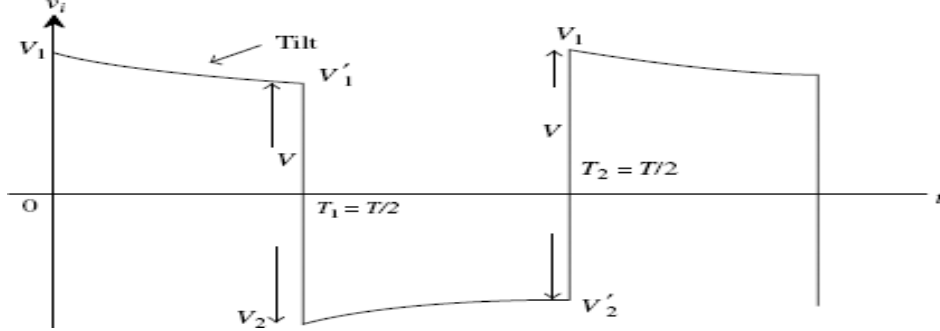
As the area under the output waveform over one cycle represents the DC component in the output, from above Eq. it is evident that the DC component in the steady-state is always zero. Now let us

consider the response of the high-pass RC circuit for a square-wave input for different values of the time constant τ , as shown in below Fig.

As is evident from the waveform in Fig.(b), there is no appreciable distortion in the output if τ is large. The output is almost the same as the input except for the fact that there is no DC component in the output. As τ decreases, as in Fig. (c), there is a tilt in the positive duration (amplitude decreases from V_1 to V_1' during the period 0 to T_1) and there is also a tilt in the negative duration (amplitude increases from V_2 to V_2' during the period T_1 to T_2). A further decrease in the value of τ [see Fig. (d)] gives rise to positive and negative spikes. There is absolutely no resemblance between the signals at the input and the output. However, this condition is imposed on high-pass circuits to derive spikes. In case a pulse is required to trigger another circuit, we see that the pulses obtained either at the rising edge (positive spike) or at the trailing edge (negative spike) may be used to edge trigger a flip-flop.



Let us consider the typical response of the high-pass circuit for a square-wave input shown in Fig below



From the above fig

$$V_1' = V_1 e^{-T_1/\tau} \quad \text{and} \quad V_1' - V_2 = V$$

$$V_2' = V_2 e^{-T_2/\tau} \quad \text{and} \quad V_1 - V_2' = V$$

..... (a)

For a symmetric square wave $T_1 = T_2 = T/2$. And, because of symmetry:

$$V_1 = -V_2 \quad \text{and} \quad V_1' = -V_2' \quad \text{.....(b)}$$

From Eq (a) $V_1' - V_2 = V$

But $V_1' = V_1 e^{-T_1/\tau}$

Therefore,

$$V_1 e^{-T_1/\tau} - V_2 = V \quad \text{.....(c)}$$

From Eq (b) $V_1 = -V_2$

Substituting in Eq. (c):

$$V_1 e^{-T_1/\tau} + V_1 = V \quad = \quad V_1(1 + e^{-T_1/\tau}) = V$$

Thus

$$V_1 = \frac{V}{1 + e^{-T_1/\tau}}$$

For a symmetric square wave, as $T_1 = T_2 = T/2$, then from above Eq. (2.39) we can written as:

$$V_1 = \frac{V}{1 + e^{-T/2\tau}}$$

But

$$V_1' = V_1 e^{-T/2\tau} = \frac{V}{(1 + e^{-T/2\tau})} \times e^{-T/2\tau}$$

There is a tilt in the output waveform. The percentage tilt, P , is defined as:

$$P = \frac{V_1 - V_1'}{\frac{V}{2}} \times 100\%$$

$$P = \frac{\frac{V}{1 + e^{-T/2\tau}} - \frac{V e^{-T/2\tau}}{1 + e^{-T/2\tau}}}{\frac{V}{2}} \times 100\% = \frac{V}{1 + e^{-T/2\tau}} \frac{[1 - e^{-T/2\tau}]}{\frac{V}{2}} \times 100\%$$

$$P = \frac{(1 - e^{-T/2\tau})}{(1 + e^{-T/2\tau})} \times 200\%$$

If $T/2\tau \ll 1$,

$$e^{-T/2\tau} = 1 - \frac{T}{2\tau}$$

Therefore

$$P = \frac{1 - \left(1 - \frac{T}{2\tau}\right)}{1 + \left(1 - \frac{T}{2\tau}\right)} \times 200\% = \frac{\frac{T}{2\tau}}{2 - \frac{T}{2\tau}} \times 200\% \cong \frac{T}{2\tau} \times 100\% \text{ since } \frac{T}{2\tau} \ll 1$$

Thus, for a symmetrical square wave:

$$P = \frac{T}{2\tau} \times 100\%,$$

Above Eq tells us that the smaller the value of τ when compared to the half-period of the square wave ($T/2$), the larger is the value of P . In other words, distortion is large with small τ and is small with large τ . The lower half-power frequency, $f_1 = 1/2\pi\tau$.

Therefore,

$$\frac{1}{2\tau} = \pi f_1$$

$$\text{So } P = \pi f_1 T \times 100\%$$

Therefore

$$P = \frac{\pi f_1}{f} \times 100\% \quad \text{since } T = \frac{1}{f}$$

High pass RC circuit response to ramp input Voltage:

A waveform which is defined as: $V_i(t) = \begin{cases} 0 & \text{for } t < 0 \\ \alpha t & \text{for } t > 0 \end{cases}$

Then the output is $V_o(t) = i(t) R$

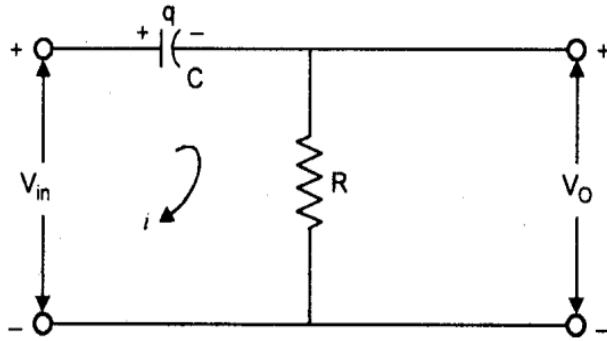


Fig. High pass RC circuit

$$\frac{dv_i(t)}{dt} = \frac{v_o(t)}{RC} + \frac{dv_o(t)}{dt}$$

Which becomes

$$\alpha = \frac{v_o(t)}{RC} + \frac{dv_o(t)}{dt}$$

This equation has the solution for $V(t)$ at $t = 0$. Taking Laplace Transform on both sides of the above equation becomes

$$\begin{aligned} \frac{\alpha}{s} &= \frac{v_o(s)}{RC} + sV_o(s) \\ &= V_o(s) \left[s + \frac{1}{RC} \right] \end{aligned}$$

$$v_o(s) = \frac{\alpha}{s \left[s + \frac{1}{RC} \right]}$$

By taking Inverse Laplace Transform,

$$v_o(t) = \alpha RC \left[1 - e^{-t/RC} \right]$$

For times ' $t \ll RC$,

$$v_o(t) = \alpha t \left[1 - \frac{t}{2RC} + \dots \right]$$

The output signal falls away slightly from the input. As a measure of the departure from linearity let us define the transmission error e_t , as the difference between input and output divided by the input. The error at a time $t = T$, is then

$$e_t = \frac{v_i(\tau) - v_o(\tau)}{v_i(\tau)}$$

$$e_t = \frac{T}{2RC} = \pi f_1 T$$

where $f_1 = 1/2\pi RC$ is again the low frequency 3-dB point.

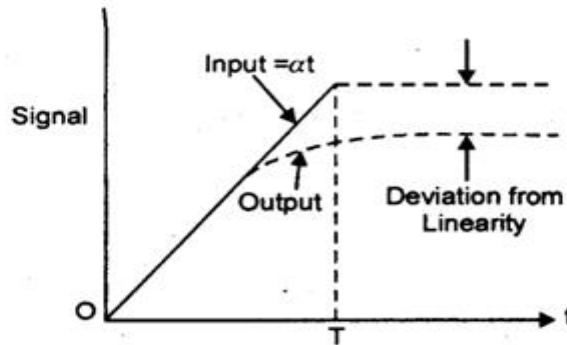
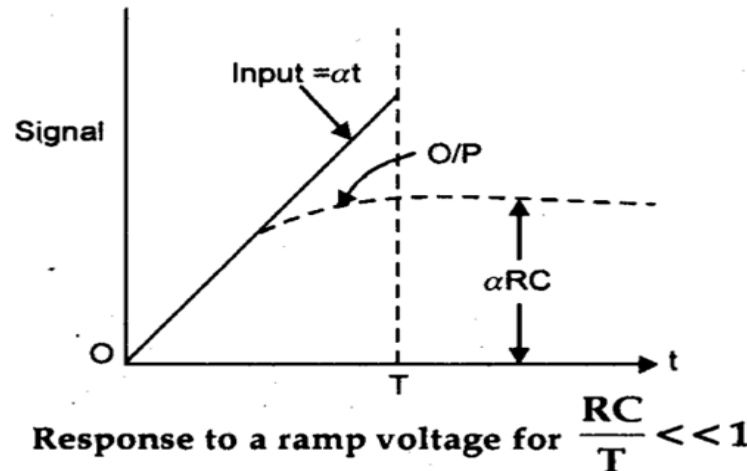


Fig. Response of a high-pass RC circuit to a ramp voltage for $\frac{RC}{T} \gg 1$



Response to a ramp voltage for $\frac{RC}{T} \ll 1$

DIFFERENTIATORS

Sometimes, a square wave may need to be converted into sharp positive and negative spikes (pulses of short duration). By eliminating the positive spikes, we can generate a train of negative spikes and vice-versa. The pulses so generated may be used to trigger a multivibrator. In such cases, a differentiator is used. If in a circuit, the output is a differential of the input signal, then the circuit is called a differentiator.

A High-pass RC Circuit as a Differentiator

If the time constant of the high-pass RC circuit, shown in Fig. 1.1(a), is much smaller than the time period of the input signal, then the circuit behaves as a differentiator. If T is to be large when compared to τ , then the frequency must be small. At low frequencies, XC is very large when compared to R . Therefore, the voltage drop across R is very small when compared to the drop across C .

$$v_i = \frac{1}{C} \int idt + iR$$

But $iR = v_o$ is small. Therefore,

$$v_i = \frac{1}{C} \int idt \quad \text{or} \quad v_i = \frac{1}{\tau} \int v_o dt \quad (\text{since } i = V_o/R)$$

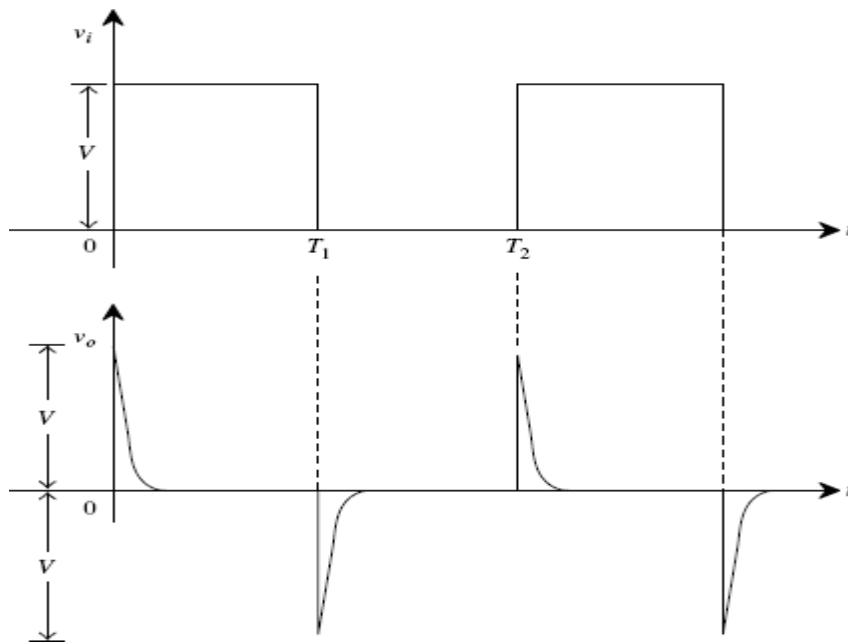


FIGURE: The output of a differentiator

Differentiating:

$$\frac{dv_i}{dt} = \frac{v_o}{\tau}$$

$$v_o = \tau \frac{dv_i}{dt}$$

Therefore

$$v_o \propto \frac{dv_i}{dt}$$

Thus, from above Eq., it can be seen that the output is proportional to the differential of the input signal.

THE LOW-PASS RC CIRCUIT

Figure 1.1 shows a low-pass RC circuit. A low-pass circuit is a circuit, which transmits only low-frequency signals and attenuates or stops high-frequency signals.

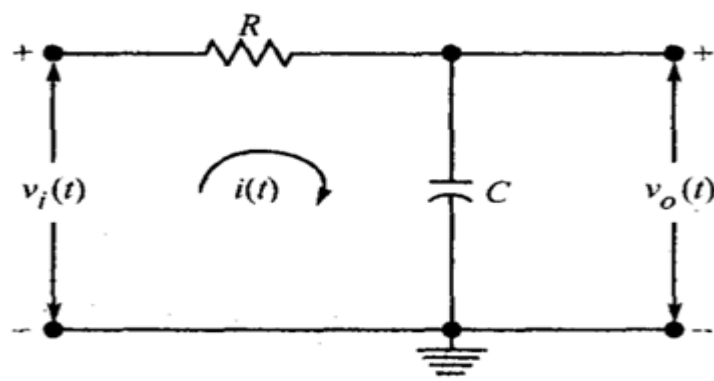


Fig The low-pass RC circuit.

At zero frequency, the reactance of the capacitor is infinity (i.e. the capacitor acts as an open circuit) so the entire input appears at the output, i.e. the input is transmitted to the output with zero attenuation. So the output is the same as the input, i.e. the gain is unity. As the frequency increases the capacitive reactance ($X_c = \frac{1}{2\pi fC}$) decreases and so the output decreases.

At very high frequencies the capacitor virtually acts as a short-circuit and the output falls to zero.

Sinusoidal Input

The Laplace transformed low-pass RC circuit is shown in Figure (a). The gain versus frequency curve of a low-pass circuit excited by a sinusoidal input is shown in Figure (b). This curve is obtained by keeping the amplitude of the input sinusoidal signal constant and varying its frequency and noting the output at each frequency. At low frequencies the output is equal to the input and hence the gain is unity. As the frequency increases, the output decreases and hence the gain decreases. The frequency at which the gain is $1/\sqrt{2}$ (≈ 0.707) of its maximum value is called the cut-off frequency. For a low-pass circuit, there is no lower cut-off frequency. It is zero itself. The upper cut-off frequency is the frequency (in the high-frequency range) at which the gain is $1/\sqrt{2}$ i.e. 70.7%, of its maximum value. The bandwidth of the low-pass circuit is equal to the upper cut-off frequency f_2 itself.

For the network shown in Figure 1.2(a), the magnitude of the steady-state gain A is given by

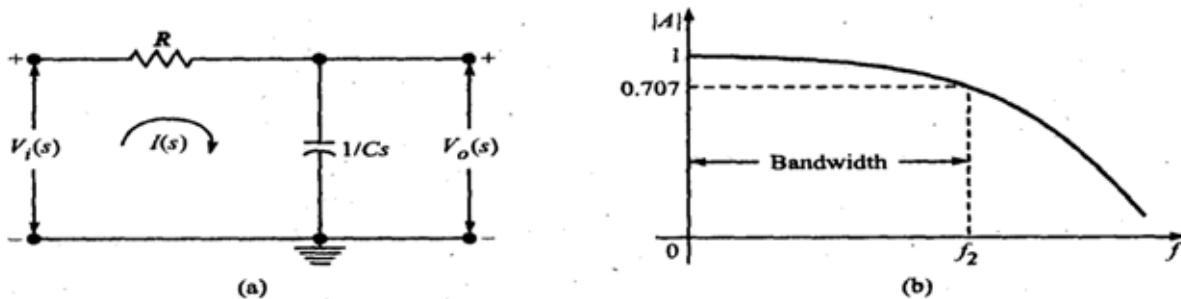


Figure (a) Laplace transformed low-pass RC circuit and (b) its frequency response.

$$A = \frac{V_o(s)}{V_i(s)} = \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}} = \frac{1}{1 + RCs} = \frac{1}{1 + j\omega RC} = \frac{1}{1 + j2\pi fRC}$$

$$\therefore |A| = \frac{1}{\sqrt{1 + (2\pi fRC)^2}}$$

$$\text{At the upper cut-off frequency } f_2, |A| = \frac{1}{\sqrt{2}}$$

$$\therefore \frac{1}{\sqrt{2}} = \frac{1}{\sqrt{1 + (2\pi f_2 RC)^2}}$$

Squaring both sides and equating the denominators,

$$2 = 1 + (2\pi f_2 RC)^2$$

∴ The upper cut-off frequency, $f_2 = \frac{1}{2\pi RC}$.

So
$$A = \frac{1}{1 + j\frac{f}{f_2}} \quad \text{and} \quad |A| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_2}\right)^2}}$$

The angle θ by which the output leads the input is given by

$$\theta = \tan^{-1} \frac{f}{f_2}$$

Step-Voltage Input

A step signal is one which maintains the value zero for all times $t < 0$, and maintains the value V for all times $t > 0$. The transition between the two voltage levels takes place at $t = 0$ and is accomplished in an arbitrarily small time interval. Thus, in Figure (a), $v_i = 0$ immediately before $t = 0$ (to be referred to as time $t = 0^-$) and $v_i = V$, immediately after $t = 0$ (to be referred to as time $t = 0^+$). In the low-pass RC circuit shown in Figure 1.1, if the capacitor is initially uncharged, when a step input is applied, since the voltage across the capacitor cannot change instantaneously, the output will be zero at $t = 0$, and then, as the capacitor charges, the output voltage rises exponentially towards the steady-state value V with a time constant RC as shown in Figure (b).

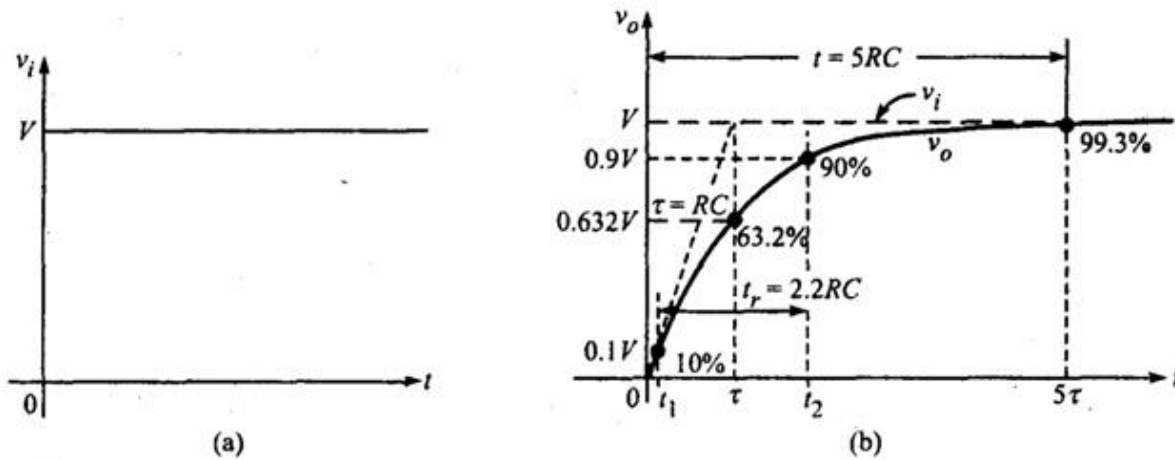


Figure (a) Step input and (b) step response of the low-pass RC circuit.

Let V' be the initial voltage across the capacitor. Writing KVL around the loop in Fig 1.1.

$$v_i(t) = Ri(t) + \frac{1}{C} \int i(t) dt$$

Differentiating this equation,

$$\frac{dv_i(t)}{dt} = R \frac{di(t)}{dt} + \frac{1}{C} i(t)$$

Since $v_i(t) = V, \quad \frac{dv_i(t)}{dt} = 0$

$\therefore 0 = R \frac{di(t)}{dt} + \frac{1}{C}i(t)$

Taking the Laplace transform on both sides,

$$0 = R [sI(s) - I(0^+)] + \frac{1}{C} I(s)$$

$\therefore I(0^+) = I(s) \left(s + \frac{1}{RC} \right)$

The initial current $I(0^+)$ is given by

$$I(0^+) = \frac{V - V'}{R}$$

$\therefore I(s) = \frac{I(0^+)}{s + \frac{1}{RC}} = \frac{V - V'}{R \left(s + \frac{1}{RC} \right)}$

and $V_o(s) = V_i(s) - I(s)R = \frac{V}{s} - \frac{(V - V')R}{R \left(s + \frac{1}{RC} \right)} = \frac{V}{s} - \frac{V - V'}{s + \frac{1}{RC}}$

Taking the inverse Laplace transform on both sides,

$$v_o(t) = V - (V - V')e^{-t/RC}$$

where V' is the initial voltage across the capacitor (V_{initial}) and V is the final voltage (V_{final}) to which the capacitor can charge.

So, the expression for the voltage across the capacitor of an RC circuit excited by a step input is given by

$$v_o(t) = V_{\text{final}} - (V_{\text{final}} - V_{\text{initial}})e^{-t/RC}$$

If the capacitor is initially uncharged, then $v_o(t) = V(1 - e^{-t/RC})$

Expression for rise time

When a step signal is applied, the rise time tr is defined as the time taken by the output voltage waveform to rise from 10% to 90% of its final value: It gives an indication of how fast the circuit can respond to a discontinuity in voltage. Assuming that the capacitor is initially uncharged, the output voltage shown in Figure (b) at any instant of time is given by

$$v_o(t) = V(1 - e^{-t/RC})$$

At $t = t_1$, $v_o(t) = 10\%$ of $V = 0.1 V$

$$\therefore 0.1V = V(1 - e^{-t_1/RC})$$

$$\therefore e^{-t_1/RC} = 0.9 \quad \text{or} \quad e^{t_1/RC} = \frac{1}{0.9} = 1.11$$

$$\therefore t_1 = RC \ln(1.11) = 0.1RC$$

At $t = t_2$, $v_o(t) = 90\%$ of $V = 0.9 V$

$$\therefore 0.9V = V(1 - e^{-t_2/RC})$$

$$\therefore e^{-t_2/RC} = 0.1 \quad \text{or} \quad e^{t_2/RC} = \frac{1}{0.1} = 10$$

$$\therefore t_2 = RC \ln 10 = 2.3RC$$

$$\therefore \text{Rise time, } t_r = t_2 - t_1 = 2.2RC$$

This indicates that the rise time t_r is proportional to the time constant RC of the circuit. The larger the time constant, the slower the capacitor charges, and the smaller the time constant, the faster the capacitor charges.

Relation between rise time and upper 3-dB frequency

We know that the upper 3-dB frequency (same as bandwidth) of a low-pass circuit is

$$f_2 = \frac{1}{2\pi RC} \quad \text{or} \quad RC = \frac{1}{2\pi f_2}$$

$$\therefore \text{Rise time, } t_r = 2.2RC = \frac{2.2}{2\pi f_2} = \frac{0.35}{f_2} = \frac{0.35}{\text{BW}}$$

Thus, the rise time is inversely proportional to the upper 3-dB frequency. The *time constant* ($T = RC$) of a circuit is defined as the time taken by the output to rise to 63.2% of the amplitude of the input step. It is same as the time taken by the output to rise to 100% of the amplitude of the input step, if the initial slope of rise is maintained. See Figure (b). The Greek letter τ is also employed as the symbol for the time constant.

Pulse Input

The pulse shown in Figure (a) is equivalent to a positive step followed by a delayed negative step as shown in Figure (b). So, the response of the low-pass RC circuit to a pulse for times less than the pulse width tp is the same as that for a step input and is given by $v_o(t) = V(1 - e^{-t/RC})$. The responses of the low-pass RC circuit for time constant $RC \gg tp$, RC smaller than tp and RC very small compared to tp are shown in Figures (c), (d), and (e) respectively.

If the time constant RC of the circuit is very large, at the end of the pulse, the output voltage will be $V_p(t) = V(1 - e^{-tp/RC})$ and the output will decrease to zero from this value with a time constant RC as shown in Figure (c). Observe that the pulse waveform is distorted when it is passed through a linear network. The output will always extend beyond the pulse width tp , because whatever charge has accumulated across the capacitor C during the pulse cannot leak off instantaneously.

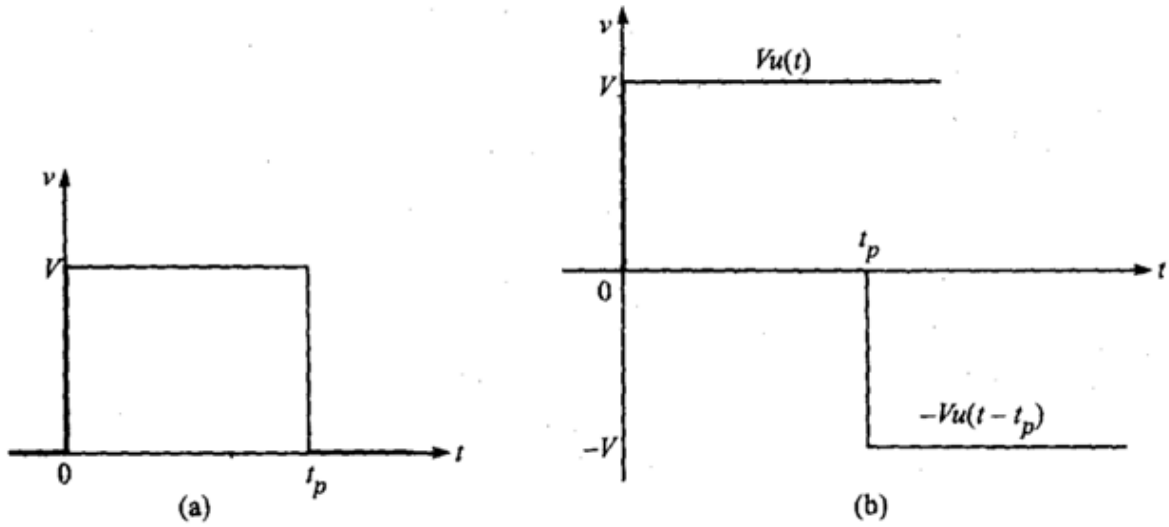


Figure (a) A pulse and (b) a pulse in terms of steps.

If the time constant RC of the circuit is very small, the capacitor charges and discharges very quickly and the rise time tr will be small and so the distortion in the wave shape is small. For minimum distortion (i.e. for preservation of wave shape), the rise time must be small compared to the pulse width tp . If the upper 3-dB frequency f_2 is chosen equal to the reciprocal of the pulse width tp , i.e. if $f_2 = 1/tp$ then $tr = 0.35tp$ and the output is as shown in Figure 1.5(b), which for many applications is a reasonable reproduction of the input. As a rule of thumb, we can say:

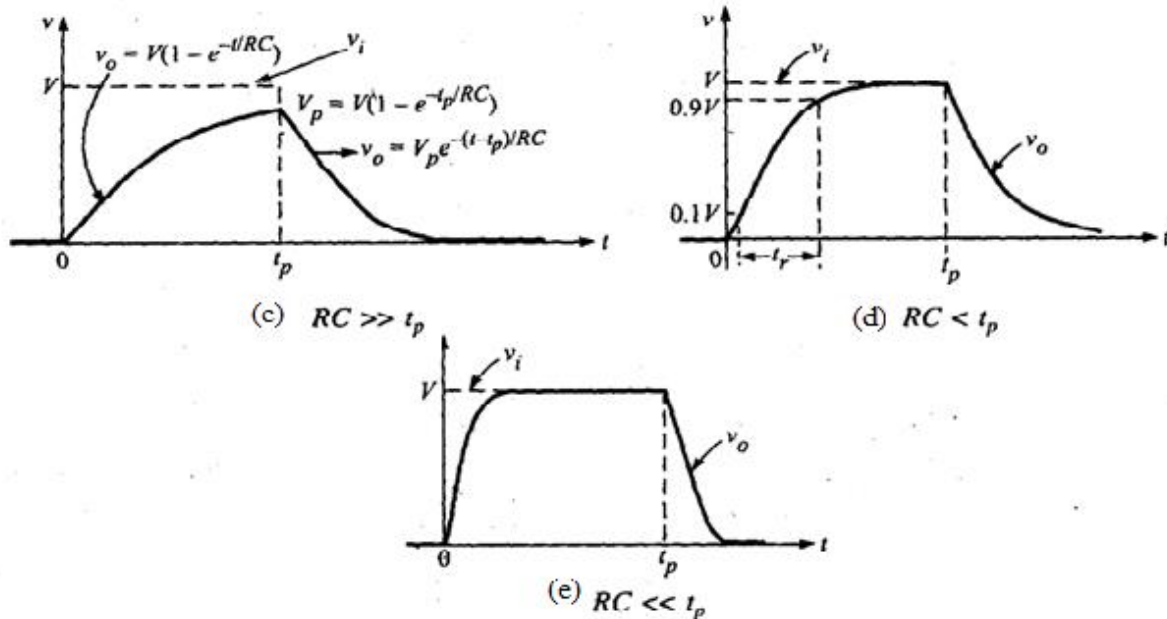


Figure Pulse response for $RC \gg tp$, $RC < tp$, and $RC \ll tp$.

A pulse shape will be preserved if the 3-dB frequency is approximately equal to the reciprocal of the pulse width.

Thus to pass a 0.25 μ s pulse reasonably well requires a circuit with an upper cut-off frequency of the order of 4 MHz.

Square-Wave Input

A square wave is a periodic waveform which maintains itself at one constant level V' with respect to ground for a time $T1$ and then changes abruptly to another level V'' , and remains constant at that level for a time $T2$, and repeats itself at regular intervals of $T = T1 + T2$. A square wave may be treated as a series of positive and negative steps.

The shape of the output waveform for a square wave input depends on the time constant of the circuit. If the time constant is very small, the rise time will also be small and a reasonable reproduction of the input may be obtained.

For the square wave shown in Figure (a), the output waveform will be as shown in Figure (b) if the time constant RC of the circuit is small compared to the period of the input waveform. In this case, the wave shape is preserved. If the time constant is comparable with the period of the input square wave, the output will be as shown in Figure (c). The output rises and falls exponentially. If the time constant is very large compared to the period of the input waveform, the output consists of exponential sections, which are essentially linear as indicated in Figure (d). Since the average voltage across R is zero, the dc voltage at the output is the same as that of the input. This average value is indicated as V_{dc} in all the waveforms.

In Figure 1.6(c), the equation for the rising portion is

$$v_{01} = V' - (V' - V_2)e^{-t/RC}$$

where V_2 is the voltage across the capacitor at $t = 0$, and V' is the level to which the capacitor can charge.

The equation for the falling portion is

$$v_{02} = V'' - (V'' - V_1)e^{-(t - T_1)/RC}$$

where V_1 is the voltage across the capacitor at $t = T_1$ and V'' is the level to which the capacitor can discharge.

Setting $v_{01} = V_1$ at $t = T_1$,

$$V_1 = V' - (V' - V_2)e^{-T_1/RC} = V'(1 - e^{-T_1/RC}) + V_2e^{-T_1/RC}$$

Setting $v_{02} = V_2$ at $t = T_1 + T_2$,

$$V_2 = V'' - (V'' - V_1)e^{-(T_1+T_2-T_1)/RC} = V''(1 - e^{-T_2/RC}) + V_1e^{-T_2/RC}$$

Substituting this value of V_2 in the expression for V_1 ,

$$V_1 = V'(1 - e^{-T_1/RC}) + [V''(1 - e^{-T_2/RC}) + V_1e^{-T_2/RC}]e^{-T_1/RC}$$

i.e.
$$V_1 = \frac{V'(1 - e^{-T_1/RC}) + V''(1 - e^{-T_2/RC})e^{-T_1/RC}}{1 - e^{-(T_1+T_2)/RC}}$$

Similarly substituting the value of V_1 in the expression for V_2 ,

$$V_2 = \frac{V''(1 - e^{-T_2/RC}) + V'(1 - e^{-T_1/RC})e^{-T_2/RC}}{1 - e^{-(T_1+T_2)/RC}}$$

For a symmetrical square wave with zero average value,

$$T_1 = T_2 = \frac{T}{2} \quad \text{and} \quad V' = -V'' = \frac{V}{2}. \quad \text{So, } V_2 \text{ will be equal to } -V_1$$

$$V_1 = \frac{\frac{V}{2}(1 - e^{-T/2RC}) - \frac{V}{2}(1 - e^{-T/2RC})e^{-T/2RC}}{1 - e^{-T/RC}}$$

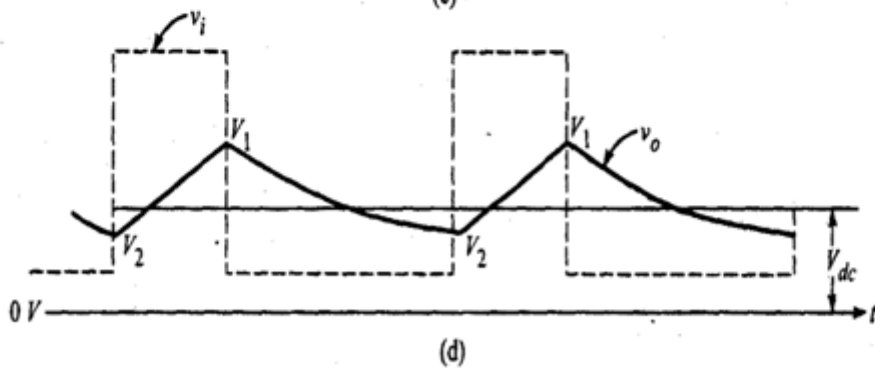
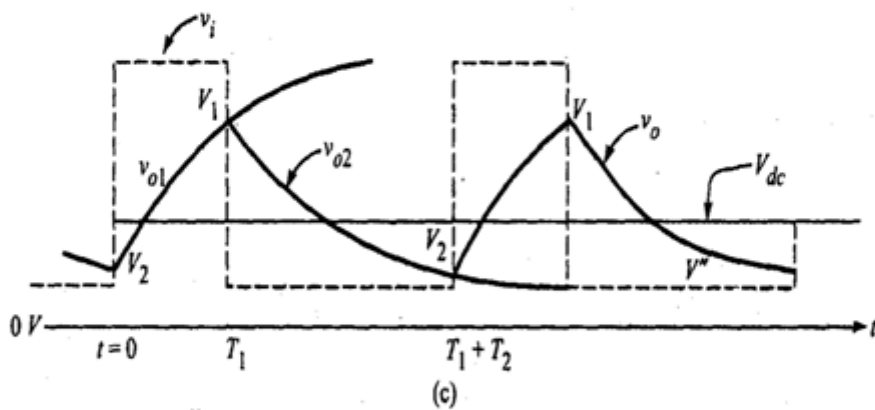
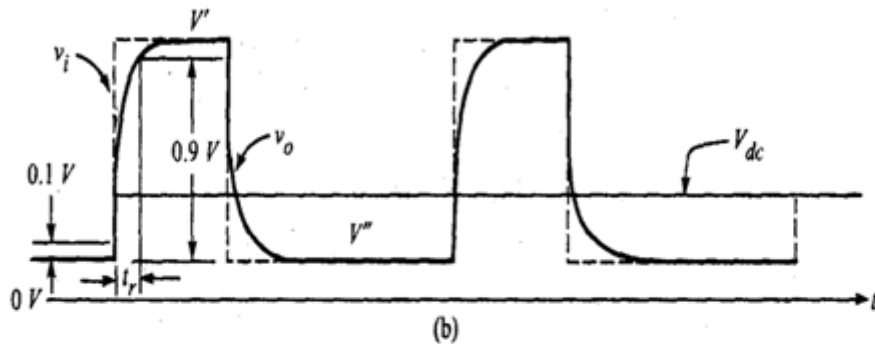
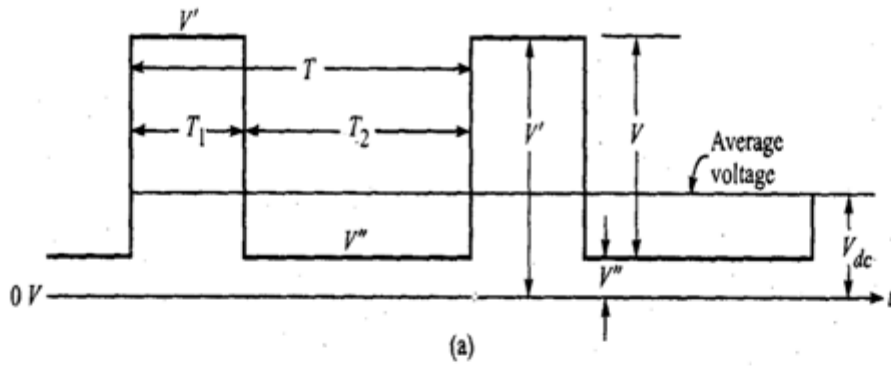


Figure Response of a low-pass RC circuit to a square wave input: (a) square-wave input wave form, (b) output waveform for $RC \ll T$, (c) output waveform for $RC = T$, and (d) output waveform for $RC \gg T$.

$$= \frac{V}{2} \frac{1 - e^{-T/2RC} - e^{-T/2RC} + e^{-T/RC}}{1 - e^{-T/RC}}$$

$$= \frac{V}{2} \frac{(1 - e^{-T/2RC})^2}{(1 + e^{-T/2RC})(1 - e^{-T/2RC})}$$

$$= \frac{V}{2} \left(\frac{1 - e^{-T/2RC}}{1 + e^{-T/2RC}} \right)$$

$$= \frac{V}{2} \left(\frac{e^{T/2RC} - 1}{e^{T/2RC} + 1} \right)$$

$$= \frac{V}{2} \left(\frac{e^{2x} - 1}{e^{2x} + 1} \right) = \frac{V}{2} \tanh x$$

where $x = \frac{T}{4RC}$ and T is the period of the square wave.

$$\text{Now, } V_2 = -V_1 = -\frac{V}{2} \left(\frac{1 - e^{-T/2RC}}{1 + e^{-T/2RC}} \right) = \frac{V}{2} \left(\frac{1 - e^{T/2RC}}{1 + e^{T/2RC}} \right)$$

Ramp Input

When a low-pass RC circuit shown in Figure is excited by a ramp input, i.e.

$$v_i(t) = \alpha t, \text{ where } \alpha \text{ is the slope of the ramp}$$

$$\text{we have, } V_i(s) = \frac{\alpha}{s^2}$$

From the frequency domain circuit of Figure (a), the output is given by

$$\begin{aligned} V_o(s) &= V_i(s) \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}} = \frac{\alpha}{s^2} \cdot \frac{1}{1 + RCs} = \frac{\alpha}{RC} \frac{1}{s^2 \left(s + \frac{1}{RC} \right)} \\ &= \frac{\alpha}{RC} \left[\frac{-(RC)^2}{s} + \frac{RC}{s^2} + \frac{(RC)^2}{s + \frac{1}{RC}} \right] \end{aligned}$$

$$\text{i.e. } V_o(s) = \frac{-\alpha RC}{s} + \frac{\alpha}{s^2} + \frac{\alpha RC}{s + \frac{1}{RC}}$$

Taking the inverse Laplace transform on both sides,

$$\begin{aligned} v_o(t) &= -\alpha RC + \alpha t + \alpha RC e^{-t/RC} \\ &= \alpha(t - RC) + \alpha RC e^{-t/RC} \end{aligned}$$

If the time constant RC is very small, $e^{-t/RC} \approx 0$

$$\therefore v_o(t) = \alpha(t - RC)$$

When the time constant is very small relative to the total ramp time T , the ramp will be transmitted with minimum distortion. The output follows the input but is delayed by one time constant RC from the input (except near the origin where there is distortion) as shown in Figure (a). If the time constant is large compared with the sweep duration, i.e. if $RC/T \gg 1$, the output will be highly distorted as shown in Figure (b).

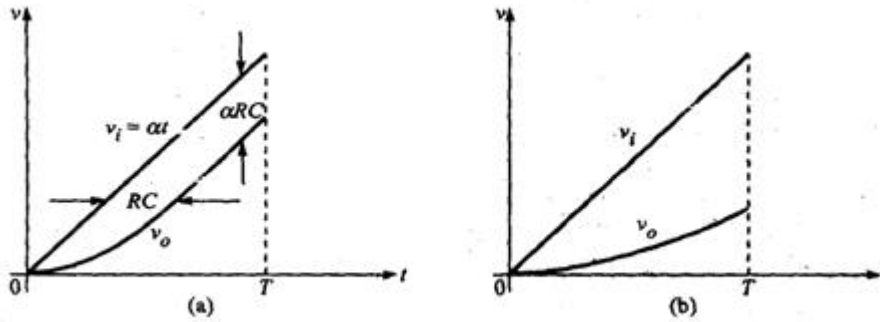


Figure Response of a low-pass RC circuit for a ramp input for (a) $RC/T \ll 1$ and (b) $RC/T \gg 1$.

Expanding $e^{-t/RC}$ in to an infinite series in t/RC in the above equation for $v_o(t)$,

$$\begin{aligned} v_o(t) &= \alpha(t - RC) + \alpha RC \left(1 - \frac{t}{RC} + \left(\frac{t}{RC} \right)^2 \frac{1}{2!} - \left(\frac{t}{RC} \right)^3 \frac{1}{3!} + \dots \right) \\ &= \alpha t - \alpha RC + \alpha RC - \alpha t + \frac{\alpha t^2}{2RC} - \dots \\ &\approx \frac{\alpha t^2}{2RC} = \frac{\alpha}{RC} \left(\frac{t^2}{2} \right) \end{aligned}$$

This shows that a quadratic response is obtained for a linear input and hence the circuit acts as an integrator for $RC/T \gg 1$.

The transmission error e_t for a ramp input is defined as the difference between the input and the output divided by the input at the end of the ramp, i.e. at $t = T$.

For $RC/T \ll 1$,

$$\begin{aligned} e_t &= \frac{\alpha t - (\alpha t - \alpha RC)}{\alpha t} \Big|_{t=T} \\ &= \frac{\alpha RC}{\alpha T} = \frac{RC}{T} = \frac{1}{2\pi f_2 T} \end{aligned}$$

where f_2 is the upper 3-dB frequency. For example, if we desire to pass a 2 ms pulse with less than 0.1% error, the above equation yields $f_2 > 80$ kHz and $RC < 2$ μ s.

THE LOW-PASS RC CIRCUIT AS AN INTEGRATOR

If the time constant of an RC low-pass circuit is very large, the capacitor charges very slowly and so almost all the input voltage appears across the resistor for small values of time.

$$v_o(t) = \frac{1}{C} \int i(t) dt = \frac{1}{C} \int \frac{v_i(t)}{R} dt = \frac{1}{RC} \int v_i(t) dt$$

Hence the output is the integral of the input, i.e. if $v_i(t) = \alpha t$, then

$$v_o(t) = \frac{\alpha t^2}{2RC}$$

As time increases, the voltage drop across C does not remain negligible compared with that across R and the output will not remain the integral of the input. The output will change from a quadratic to a linear function of time.

If the time constant of an RC low-pass circuit is very large in comparison with the time required for the input signal to make an appreciable change, the circuit acts as an integrator.

A criterion for good integration in terms of steady-state analysis is as follows: The low-pass circuit acts as an integrator provided the time constant of the circuit $RC > 15T$, where T is the period of

the input sine wave. When $RC > 15T$, the input sinusoid will be shifted at least by 89.4° (instead of the ideal 90° shift required for integration) when it is transmitted through the network.

An RC integrator converts a square wave into a triangular wave. Integrators are almost invariably preferred over differentiators in analog computer applications for the following reasons:

1. It is easier to stabilize an integrator than a differentiator because the gain of an integrator decreases with frequency whereas the gain of a differentiator increases with frequency.
2. An integrator is less sensitive to noise voltages than a differentiator because of its limited bandwidth.
3. The amplifier of a differentiator may overload if the input waveform changes very rapidly.
4. It is more convenient to introduce initial conditions in an integrator.

Attenuators

An attenuator is a circuit that reduces the amplitude of the signal by a finite amount. A simple resistance attenuator is represented in the below Fig. The output of the attenuator shown in Fig. is given by the relation:

$$v_o = v_i \times \frac{R_2}{R_1 + R_2} = \alpha v_i$$

From this equation, it is evident that the output is smaller than the input, which is the main purpose of an attenuator—to reduce the amplitude of the signal. Attenuators are used when the signal amplitude is very large. Let us measure a voltage, say, 5000 V, using a CRO; such a large voltage may not be handled by the amplifier in a CRO. Therefore, to be able to measure such a voltage we first attenuate the voltage by a known amount, say by a factor of 10 ($\alpha = 0.1$), so that the voltage that is actually connected to the CRO is only 500 V. The output of the attenuator is thus reduced depending on the choice of R_1 and R_2 .

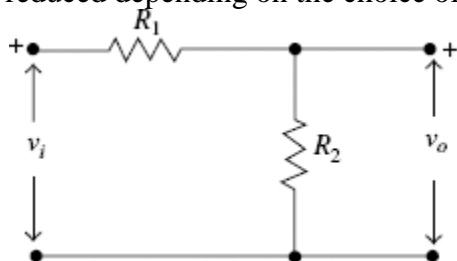
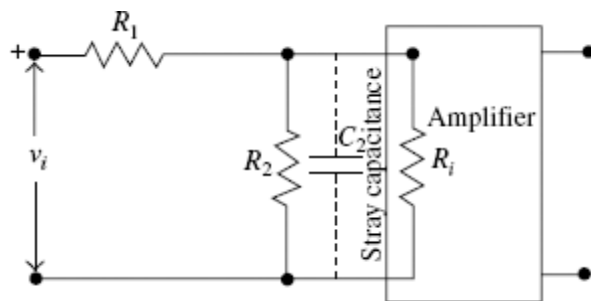


FIGURE: A resistance attenuator



FIGURE(a): The attenuator output connected to amplifier input

Uncompensated Attenuators

If the output of an attenuator is connected as input to an amplifier with a stray capacitance C_2 and input resistance R_i , as shown in Fig.(a).

Consider the parallel combination of R_2 and R_i . If the amplifier input is not to load the attenuator output, then R_i should always be significantly greater than R_2 . The attenuator circuit is now shown in Fig.(b).

Reducing the two-loop network into a single-loop network by Thevenizing:

$$V_{Th} = v_i \times \frac{R_2}{R_1 + R_2} = \alpha v_i \quad \text{where} \quad \alpha = \frac{R_2}{R_1 + R_2}$$

And $R_{th} = R_1 || R_2$

Hence, the circuit in Fig.(b) reduces to that shown in Fig. (c).

When the input αv_i is applied to this low-pass RC circuit, the output will not reach the steady-state value instantaneously. If, for the above circuit, $R_1 = R_2 = 1 \text{ M}\Omega$ and $C_2 = 20 \text{ nF}$, the rise time is:

$$tr = 2.2 R_{th} C_2 = 2.2 \times 0.5 \times 10^6 \times 20 \times 10^{-9}$$

$$tr = 22\text{ms}$$

This means that after a time interval of approximately 22ms after the application of the input αv_i to the circuit, the output reaches the steady-state value. This is an abnormally long delay. An attenuator of this type is called an uncompensated attenuator, i.e., its output is dependent on frequency.

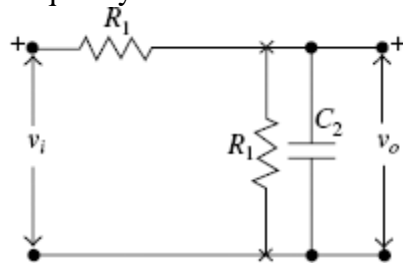


FIGURE (b): The attenuator, considering the stray capacitance at the amplifier input

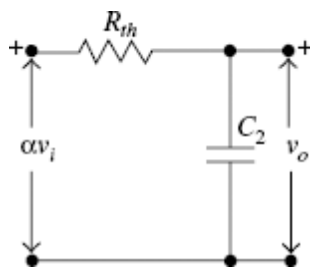


FIGURE (c): An uncompensated attenuator

Compensated Attenuators

To make the response of the attenuator independent of frequency, the capacitor C_1 is connected across R_1 . This attenuator now is called a compensated attenuator shown in below Fig. (d). This circuit in Fig. (d) is redrawn as shown in below Fig. (e).

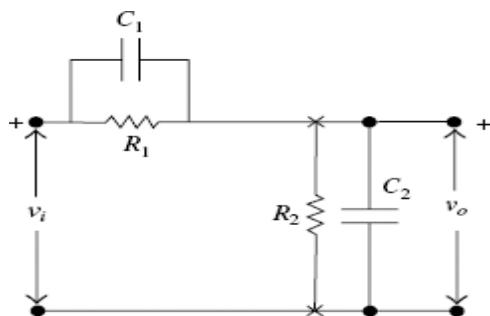


FIGURE (d) A compensated attenuator

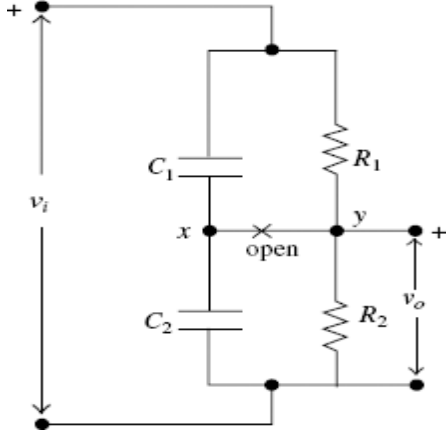


FIGURE (e) Redrawn circuit of Fig (d)

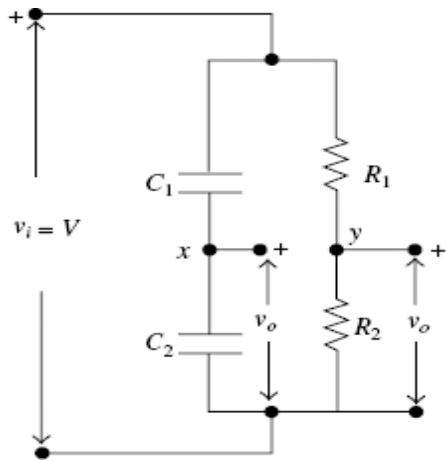


FIGURE (f) The compensated attenuator open-circuiting the xy branch

In Figs. (d) and (e), R_1 , R_2 , C_1 , C_2 form the four arms of the bridge. The bridge is said to be balanced when $R_1C_1 = R_2C_2$, in which case no current flows in the branch xy . Hence, for the purpose of computing the output, the branch xy is omitted. The resultant circuit is shown in Fig. (f).

When a step voltage with $v_i = V$ is applied as an input, the output is calculated as follows: At $t = 0^+$, the capacitors do not allow any sudden changes in the voltage; as the input changes, the output should also change abruptly, depending on the values of C_1 and C_2 .

$$v_o(0^+) = V \frac{C_1}{C_1 + C_2}$$

Thus, the initial output voltage is determined by C_1 and C_2 . As $t \rightarrow \infty$, the capacitors are fully charged and they behave as open circuits for dc. Hence, the resultant output is:

$$v_o(\infty) = V \frac{R_2}{R_1 + R_2}$$

Perfect compensation is obtained if, $v_o(0^+) = v_o(\infty)$

From this using above Eqs., we get:

$$\frac{C_1}{C_1 + C_2} V = V \frac{R_2}{R_1 + R_2}$$

and the output is αv_i .

$$C_1 R_1 = C_2 R_2 \quad \text{or}$$

$$C_1 = (R_2/R_1)C_2 = C_p$$

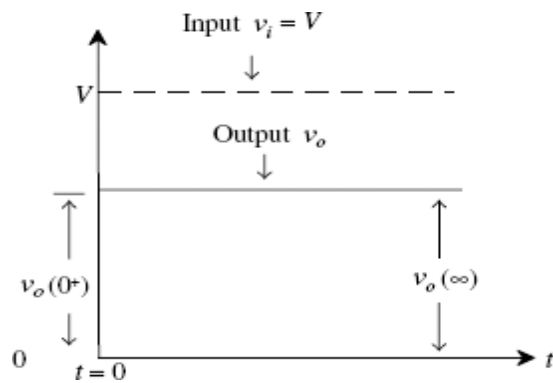


FIGURE (g) A perfectly compensated attenuator ($C_1 = C_2$)

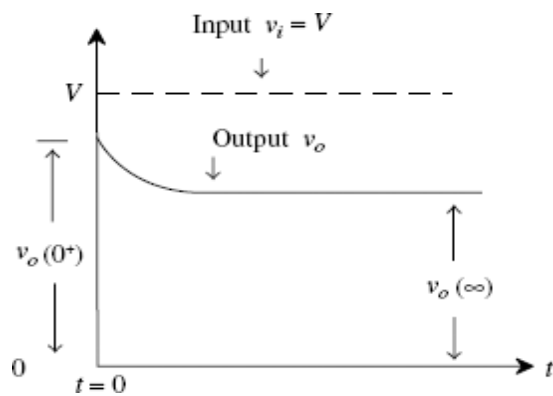


FIGURE (h) An over-compensated attenuator ($C_1 > C_2$)

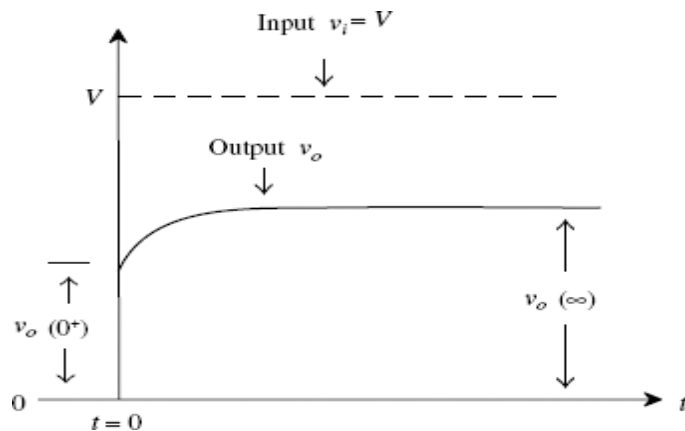


FIGURE (i) An under-compensated attenuator ($C_1 < C_2$)

Let us consider the following circuit conditions:

1. When $C_1 = C_p$, the attenuator is a perfectly compensated attenuator.
2. When $C_1 > C_p$, it is an over-compensated attenuator.
3. When $C_1 < C_p$, it is an under-compensated attenuator.

The response of the attenuator to a step input under these three conditions is shown in Figs. (g),(h) and (i), respectively.

In the attenuator circuit, as at $t = 0+$, the capacitors C_1 and C_2 behave as short circuits, the current must be infinity. But impulse response is impossible as the generator, in practice, has a finite source resistance, not ideally zero. Now consider the compensated attenuator with source resistance R_s [see Fig. (j)].

If the xy loop is open for a balanced bridge, Thevenizing the circuit, the Thevenin voltage source and its internal resistance and R' are calculated using Fig. (k).

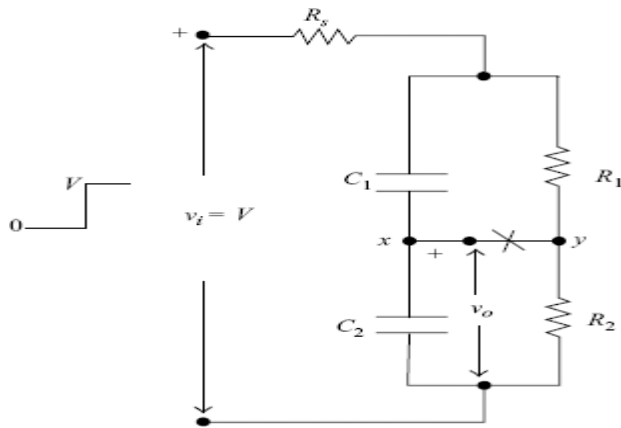


FIGURE (j) The attenuator taking the source resistance into account

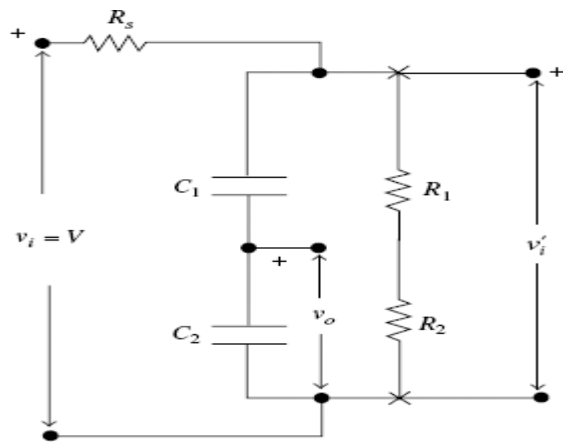


FIGURE (k) The circuit used to calculate the Thevenin voltage source and its internal resistance

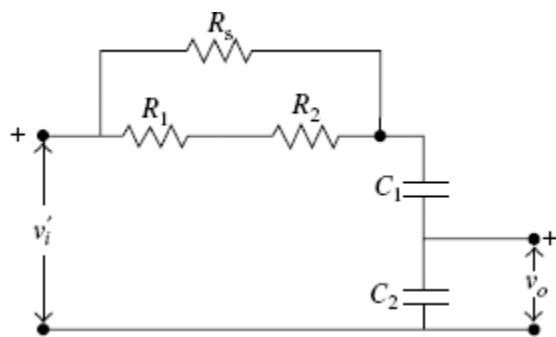


FIGURE (i) Redrawn circuit of Fig.(k)

The value of Thevenin voltage source is:

$$v_i' = \frac{v_i(R_1 + R_2)}{R_s + R_1 + R_2}$$

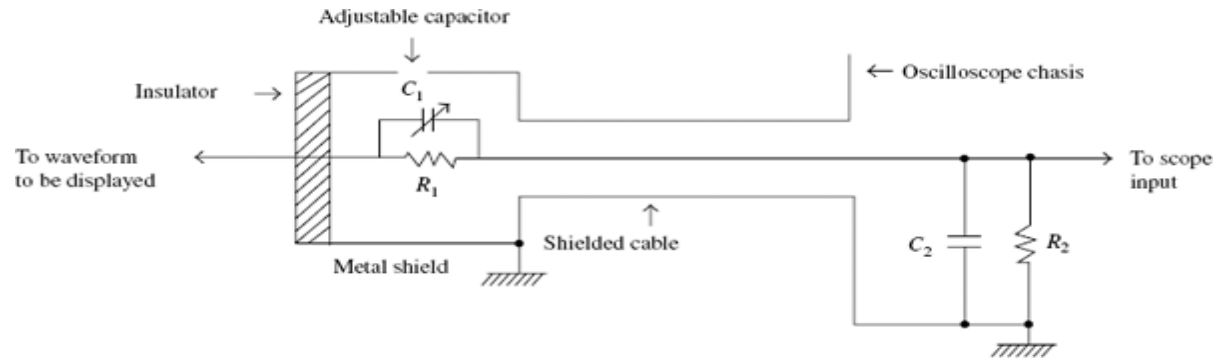
and its internal resistance is:

$$R' = \frac{R_s(R_1 + R_2)}{R_s + R_1 + R_2}$$

The above circuit now reduces to that shown in above Fig. (i). Usually $R_s \parallel (R_1 + R_2) \approx R_s$.

This is a low-pass circuit with time constant $\tau_s = R_s C_s$, where C_s is the series combination of C_1 and C_2 ; $C_s = C_1 C_2 / (C_1 + C_2)$. The output of the attenuator is an exponential with time constant τ_s ; and if τ_s is small, the output almost follows the input.

A perfectly compensated attenuator is sometimes used to reduce the signal amplitude when the signal is connected to a CRO to display a waveform. A typical CRO probe may be represented as in below Fig.



RL circuits:

RL High pass filter: It is an electronic circuit which allows all the inputs with frequencies greater than a particular frequency called the cut-off frequency to pass through it.

Transfer Function

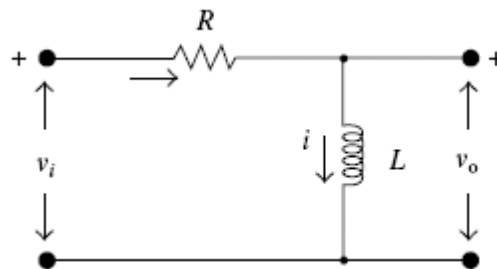


Fig. RL High Pass Circuit

$$v_o(\omega) = v_i(\omega) \cdot \frac{j\omega L}{R + j\omega L}$$

$$H(\omega) = \frac{v_o(\omega)}{v_i(\omega)} = \frac{j\omega L}{R + j\omega L}$$

$$|H(\omega)| = \left| \frac{v_o(\omega)}{v_i(\omega)} \right| = \left| \frac{j\omega L}{R + j\omega L} \right|$$

$$|H(\omega)| = \frac{\omega L}{\sqrt{R^2 + \omega^2 L^2}}$$

$$|H(\omega)| = \frac{\omega L / R}{\sqrt{1 + \omega^2 (L/R)^2}}$$

$$|H(\omega)| = \frac{2\pi fL/R}{\sqrt{1 + 4\pi^2 f^2 (L/R)^2}}$$

Frequency Response:

$$\text{If } f_l = \frac{1}{2\pi(L/R)} \quad |H(\omega)| = \frac{f/f_l}{\sqrt{1+(f/f_l)^2}}$$

$$\text{If } f \ll f_l \quad (f/f_l)^2 \ll 1 \quad |H(\omega)| = f/f_l$$

As frequency increases $|H(\omega)|$ also increases and the rate of increase is 20dB/decade.

$$\text{If } f = f_l \quad (f/f_l)^2 = 1 \quad |H(\omega)| = \frac{1}{\sqrt{2}}$$

$$\text{If } f \gg f_l \quad (f/f_l)^2 \gg 1 \quad |H(\omega)| = 1$$

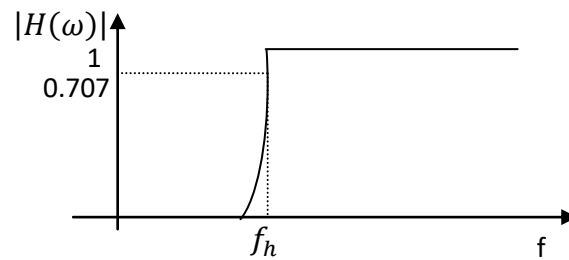


Fig. Frequency Response

The frequency response indicates that the frequencies below f_l will be blocked by the circuit and the frequencies above f_l will be transmitted. This shows that the circuit is indeed a Highpass filter.

Response of RL Highpass filter to a step input:

$$v_i(t) = Au(t)$$

$$v_i(s) = \frac{A}{s}$$

$$v_0(s) = v_i(s) \frac{Ls}{R + Ls}$$

$$= \frac{A}{s} \frac{Ls}{R + Ls}$$

$$= A \frac{1}{R/L + s}$$

$$v_0(s) = A \frac{1}{s + R/L}$$

$$v_0(t) = A \cdot e^{-\frac{tR}{L}} u(t)$$

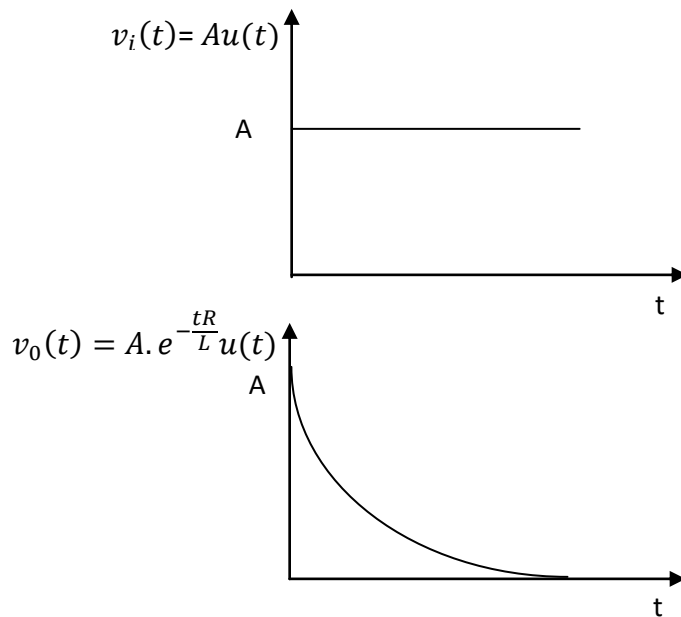


Fig. Response of RL High pass filter to a step input

RL Low pass filter: It is an electronic circuit which allows all the inputs with frequencies lesser than a particular frequency called the cut-off frequency to pass through it.

Transfer Function

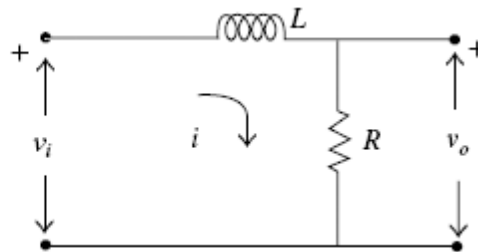


Fig. RL Low pass filter

$$v_0(\omega) = v_i(\omega) \cdot \frac{R}{R + j\omega L}$$

$$H(\omega) = \frac{v_0(\omega)}{v_i(\omega)} = \frac{R}{R + j\omega L}$$

$$|H(\omega)| = \left| \frac{v_0(\omega)}{v_i(\omega)} \right| = \left| \frac{R}{R + j\omega L} \right|$$

$$|H(\omega)| = \frac{R}{\sqrt{R^2 + \omega^2 L^2}}$$

$$|H(\omega)| = \frac{1}{\sqrt{1 + \omega^2 (L/R)^2}}$$

$$|H(\omega)| = \frac{1}{\sqrt{1 + 4\pi^2 f^2 (L/R)^2}}$$

Frequency Response:

$$\text{If } f_h = \frac{1}{2\pi\left(\frac{L}{R}\right)} \quad |H(\omega)| = \frac{1}{\sqrt{1+(f/f_h)^2}}$$

$$\text{If } f \ll f_h \quad (f/f_h)^2 \ll 1 \quad |H(\omega)| = 1$$

$$\text{If } f = f_h \quad (f/f_h)^2 = 1 \quad |H(\omega)| = \frac{1}{\sqrt{2}}$$

$$\text{If } f \gg f_h \quad (f/f_h)^2 \gg 1 \quad |H(\omega)| = f_h/f$$

As frequency increases $|H(\omega)|$ also decreases and the rate of decrease is 20dB/decade.

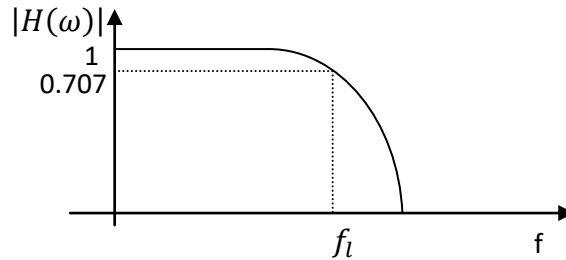


Fig. Frequency Response

The frequency response indicates that the frequencies below f_l will be transmitted by the circuit and the frequencies above f_l will be blocked. This shows that the circuit is indeed a Lowpass filter.

Response of RL Lowpass filter to a step input:

$$v_i(t) = Au(t)$$

$$v_i(s) = \frac{A}{s}$$

$$v_0(s) = v_i(s) \frac{R}{R + Ls}$$

$$= \frac{A}{s} \frac{R}{R + Ls}$$

$$= \frac{A}{s} \frac{R/L}{R/L + s}$$

$$= \frac{A1}{s} + \frac{A2}{R/L + s}$$

$$= \frac{A}{s} + \frac{-A}{R/L + s}$$

$$v_0(t) = Au(t) - A \cdot e^{-\frac{tR}{L}} u(t)$$

$$v_0(t) = A(1 - e^{-\frac{tR}{L}})u(t)$$

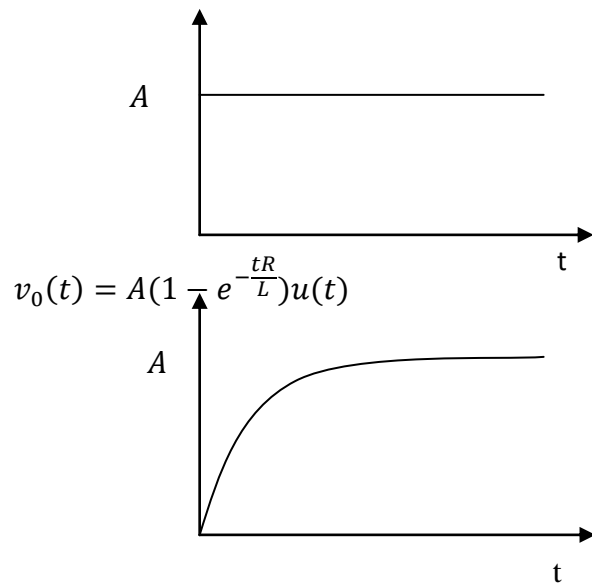


Fig. Response of RL Low pass filter to a step input

MODULE IV: NON - LINEAR WAVE SHAPING

the non-linear elements like **diodes** are used in nonlinear wave shaping circuits to get required altered outputs. Either the shape of the wave is attenuated or the dc level of the wave is altered in the Non-linear wave shaping.

The process of producing non-sinusoidal output wave forms from sinusoidal input, using non-linear elements is called as **nonlinear wave shaping**.

Clipper Circuits

A Clipper circuit is a circuit that **rejects the part** of the input wave specified while **allowing the remaining** portion. The portion of the wave above or below the cut off voltage determined is clipped off or cut off.

The clipping circuits consist of linear and non-linear elements like resistors and diodes but not energy storage elements like capacitors. These clipping circuits have many applications as they are advantageous.

- The main advantage of clipping circuits is to eliminate the unwanted noise present in the amplitudes.
- These can work as square wave converters, as they can convert sine waves into square waves by clipping.
- The amplitude of the desired wave can be maintained at a constant level.

Among the Diode Clippers, the two main types are **positive** and **negative clippers**.

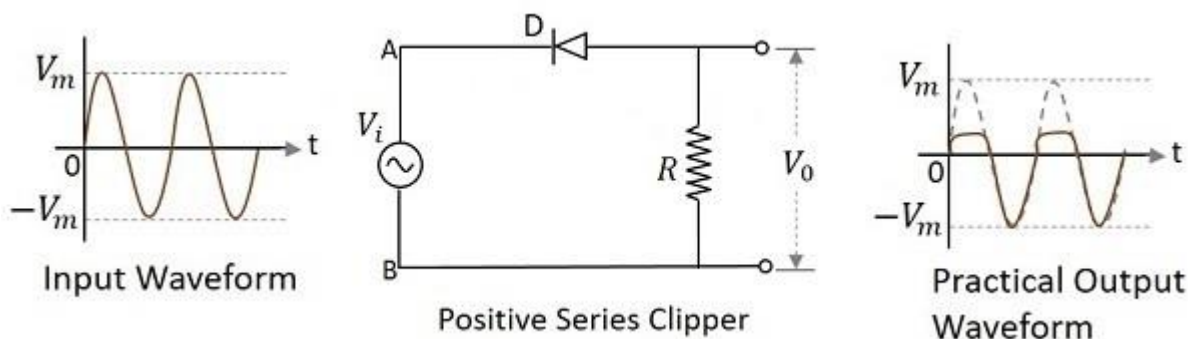
The Clipper circuit that is intended to attenuate positive portions of the input signal can be termed as a **Positive Clipper**. Among the positive diode clipper circuits, we have the following types –

- Positive Series Clipper
- Positive Series Clipper with positive V_r reference voltage
- Positive Series Clipper with negative V_r
- Positive Shunt Clipper
- Positive Shunt Clipper with positive V_r
- Positive Shunt Clipper with negative V_r

Let us discuss each of these types in detail.

Positive Series Clipper

A Clipper circuit in which the diode is connected in series to the input signal and that attenuates the positive portions of the waveform, is termed as **Positive Series Clipper**. The following figure represents the circuit diagram for positive series clipper.

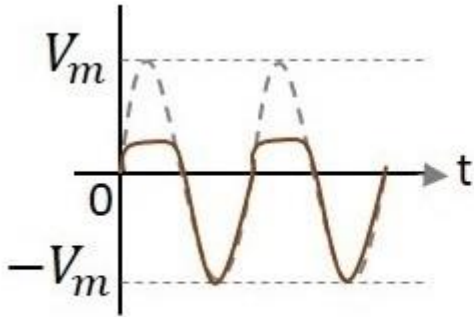


Positive Cycle of the Input – When the input voltage is applied, the positive cycle of the input makes the point A in the circuit positive with respect to the point B. This makes the diode reverse biased and hence it behaves like an open switch. Thus the voltage across the load resistor becomes zero as no current flows through it and hence V_O will be zero.

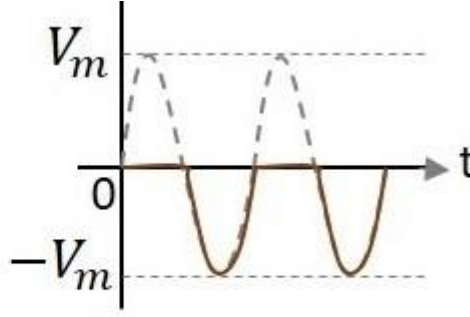
Negative Cycle of the Input – The negative cycle of the input makes the point A in the circuit negative with respect to the point B. This makes the diode forward biased and hence it conducts like a closed switch. Thus the voltage across the load resistor will be equal to the applied input voltage as it completely appears at the output V_O .

Waveforms

In the above figures, if the waveforms are observed, we can understand that only a portion of the positive peak was clipped. This is because of the voltage across V_O . But the ideal output was not meant to be so. Let us have a look at the following figures.



Practical Output Waveform

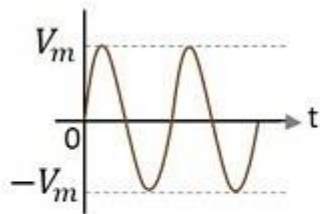


Ideal Output Waveform

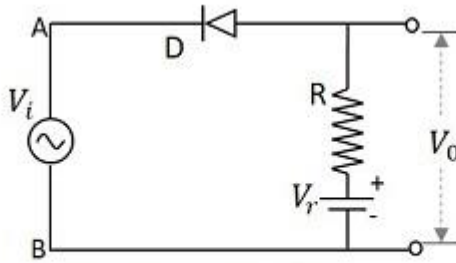
Unlike the ideal output, a bit portion of the positive cycle is present in the practical output due to the diode conduction voltage which is $0.7v$. Hence there will be a difference in the practical and ideal output waveforms.

Positive Series Clipper with positive V_r

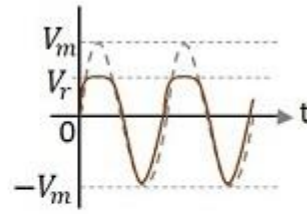
A Clipper circuit in which the diode is connected in series to the input signal and biased with positive reference voltage V_r and that attenuates the positive portions of the waveform, is termed as **Positive Series Clipper with positive V_r** . The following figure represents the circuit diagram for positive series clipper when the reference voltage applied is positive.



Input Waveform



Positive Series Clipper with positive V_r



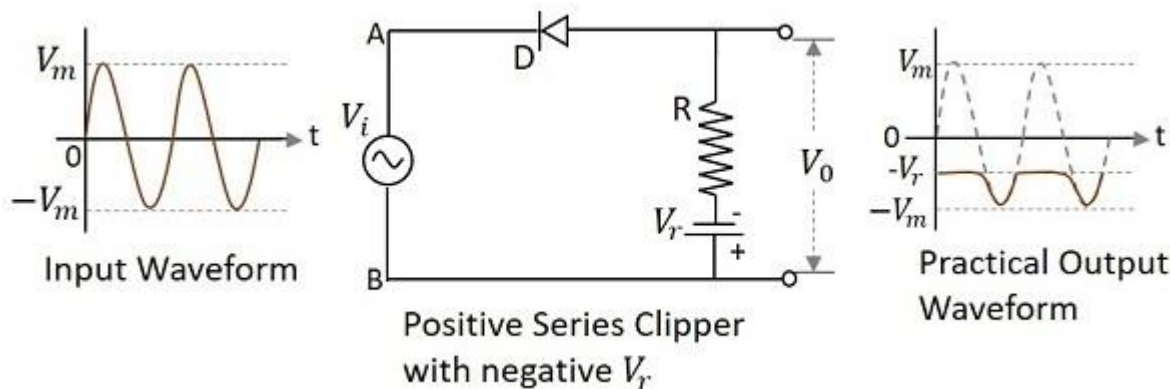
Practical Output Waveform

During the positive cycle of the input the diode gets reverse biased and the reference voltage appears at the output. During its negative cycle, the diode gets forward biased and conducts like a closed switch. Hence the output waveform appears as shown in the above figure.

Positive Series Clipper with negative V_r

A Clipper circuit in which the diode is connected in series to the input signal and biased with negative reference voltage V_r and that attenuates the positive portions of the waveform, is

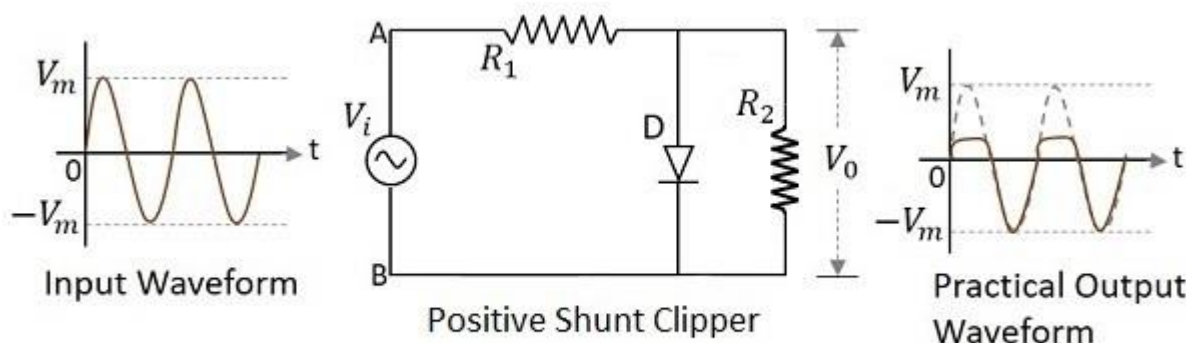
termed as **Positive Series Clipper with negative V_r** . The following figure represents the circuit diagram for positive series clipper, when the reference voltage applied is negative.



During the positive cycle of the input the diode gets reverse biased and the reference voltage appears at the output. As the reference voltage is negative, the same voltage with constant amplitude is shown. During its negative cycle, the diode gets forward biased and conducts like a closed switch. Hence the input signal that is greater than the reference voltage, appears at the output.

Positive Shunt Clipper

A Clipper circuit in which the diode is connected in shunt to the input signal and that attenuates the positive portions of the waveform, is termed as **Positive Shunt Clipper**. The following figure represents the circuit diagram for positive shunt clipper.

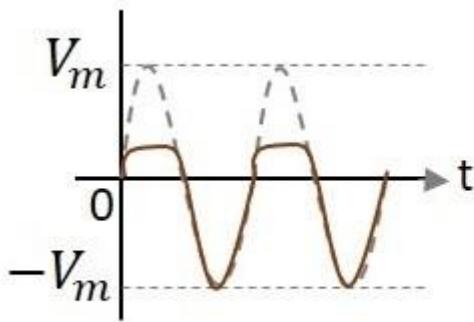


Positive Cycle of the Input – When the input voltage is applied, the positive cycle of the input makes the point A in the circuit positive with respect to the point B. This makes the diode forward biased and hence it conducts like a closed switch. Thus the voltage across the load resistor becomes zero as no current flows through it and hence V_0 will be zero.

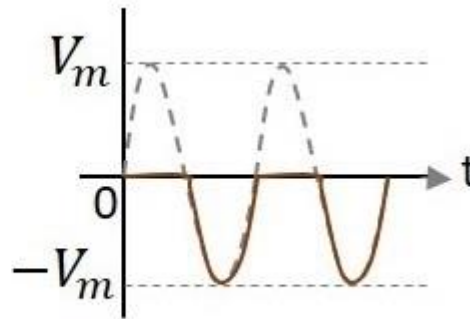
Negative Cycle of the Input – The negative cycle of the input makes the point A in the circuit negative with respect to the point B. This makes the diode reverse biased and hence it behaves like an open switch. Thus the voltage across the load resistor will be equal to the applied input voltage as it completely appears at the output V_0 .

Waveforms

In the above figures, if the waveforms are observed, we can understand that only a portion of the positive peak was clipped. This is because of the voltage across V_0 . But the ideal output was not meant to be so. Let us have a look at the following figures.



Practical Output Waveform

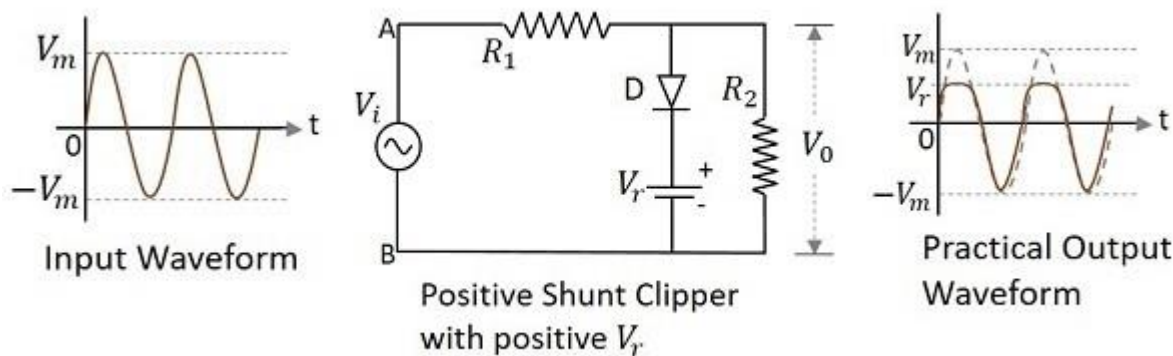


Ideal Output Waveform

Unlike the ideal output, a bit portion of the positive cycle is present in the practical output due to the diode conduction voltage which is 0.7v. Hence there will be a difference in the practical and ideal output waveforms.

Positive Shunt Clipper with positive V_r

A Clipper circuit in which the diode is connected in shunt to the input signal and biased with positive reference voltage V_r and that attenuates the positive portions of the waveform, is termed as **Positive Shunt Clipper with positive V_r** . The following figure represents the circuit diagram for positive shunt clipper when the reference voltage applied is positive.

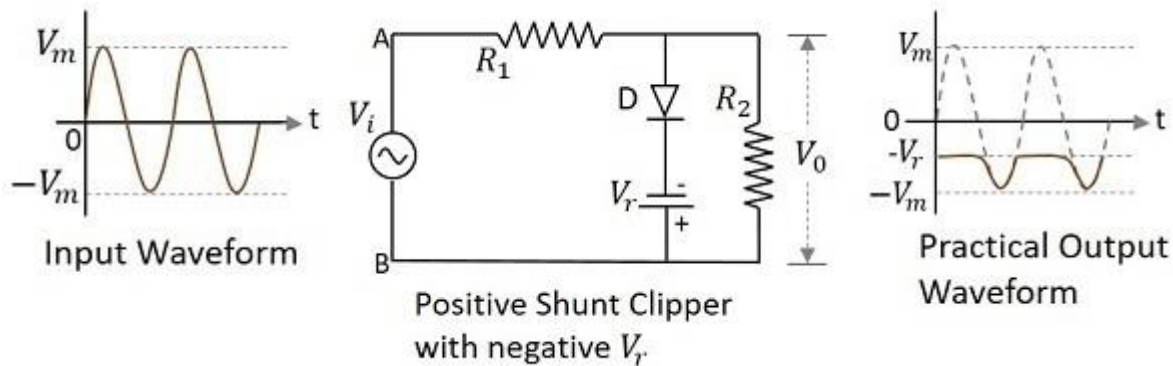


During the positive cycle of the input the diode gets forward biased and nothing but the reference voltage appears at the output. During its negative cycle, the diode gets reverse biased and behaves as an open switch. The whole of the input appears at the output. Hence the output waveform appears as shown in the above figure.

Positive Shunt Clipper with negative V_r

A Clipper circuit in which the diode is connected in shunt to the input signal and biased with negative reference voltage V_r and that attenuates the positive portions of the waveform, is termed as **Positive Shunt Clipper with negative V_r** .

The following figure represents the circuit diagram for positive shunt clipper, when the reference voltage applied is negative.



During the positive cycle of the input, the diode gets forward biased and the reference voltage appears at the output. As the reference voltage is negative, the same voltage with constant amplitude is shown. During its negative cycle, the diode gets reverse biased and behaves as an open switch. Hence the input signal that is greater than the reference voltage, appears at the output.

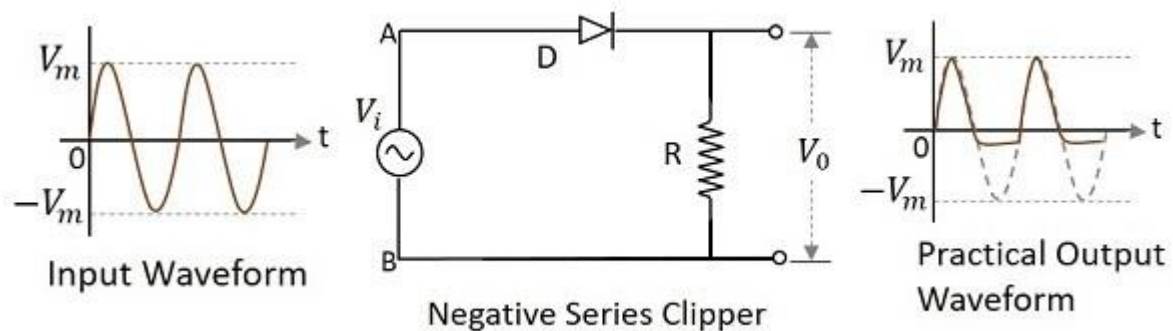
The Clipper circuit that is intended to attenuate negative portions of the input signal can be termed as a **Negative Clipper**. Among the negative diode clipper circuits, we have the following types.

- Negative Series Clipper
- Negative Series Clipper with positive V_r
- Negative Series Clipper with negative V_r
- Negative Shunt Clipper
- Negative Shunt Clipper with positive V_r
- Negative Shunt Clipper with negative V_r

Let us discuss each of these types in detail.

Negative Series Clipper

A Clipper circuit in which the diode is connected in series to the input signal and that attenuates the negative portions of the waveform, is termed as **Negative Series Clipper**. The following figure represents the circuit diagram for negative series clipper.

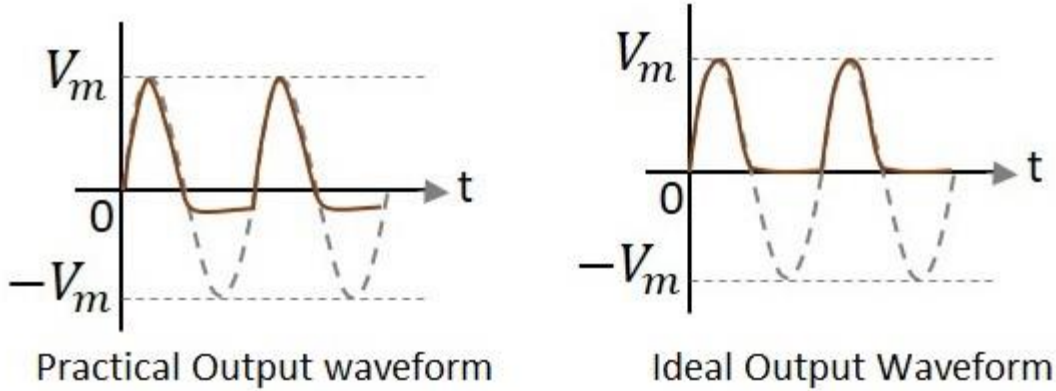


Positive Cycle of the Input – When the input voltage is applied, the positive cycle of the input makes the point A in the circuit positive with respect to the point B. This makes the diode forward biased and hence it acts like a closed switch. Thus the input voltage completely appears across the load resistor to produce the output V_0 .

Negative Cycle of the Input – The negative cycle of the input makes the point A in the circuit negative with respect to the point B. This makes the diode reverse biased and hence it acts like an open switch. Thus the voltage across the load resistor will be zero making V_0 zero.

Waveforms

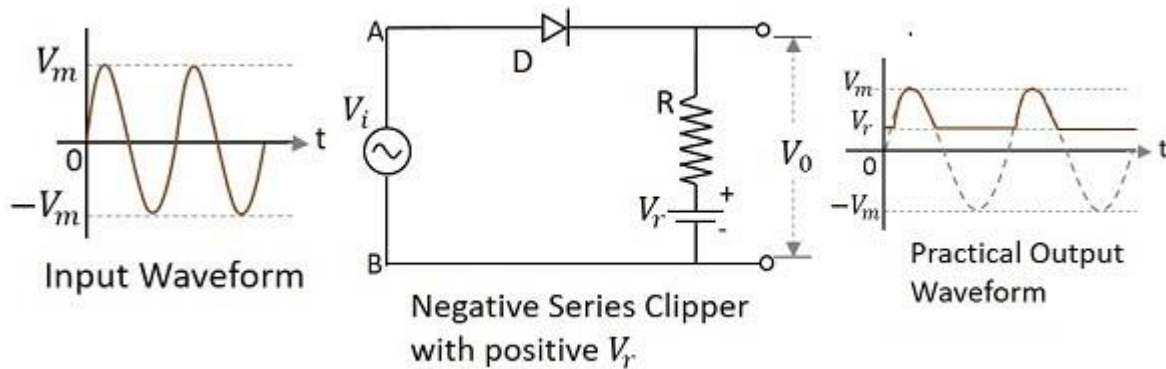
In the above figures, if the waveforms are observed, we can understand that only a portion of the negative peak was clipped. This is because of the voltage across V_0 . But the ideal output was not meant to be so. Let us have a look at the following figures.



Unlike the ideal output, a bit portion of the negative cycle is present in the practical output due to the diode conduction voltage which is $0.7v$. Hence there will be a difference in the practical and ideal output waveforms.

Negative Series Clipper with positive V_r

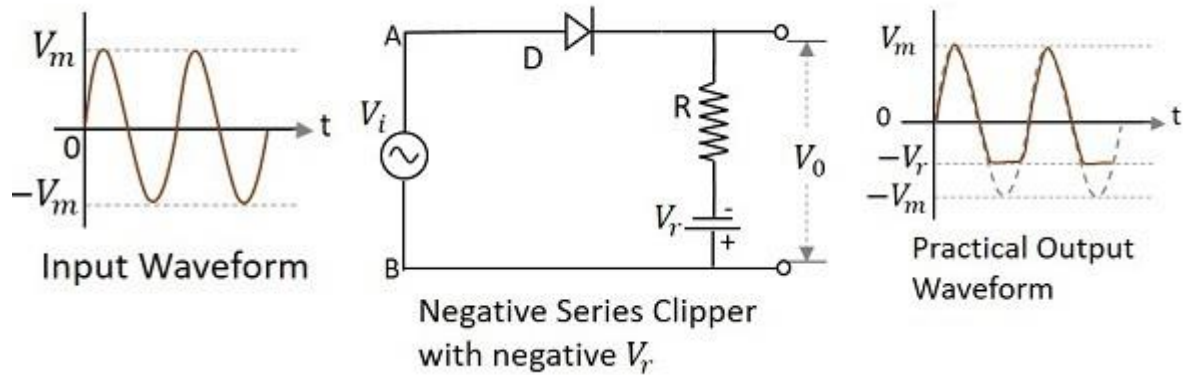
A Clipper circuit in which the diode is connected in series to the input signal and biased with positive reference voltage V_r and that attenuates the negative portions of the waveform, is termed as **Negative Series Clipper with positive V_r** . The following figure represents the circuit diagram for negative series clipper when the reference voltage applied is positive.



During the positive cycle of the input, the diode starts conducting only when the anode voltage value exceeds the cathode voltage value of the diode. As the cathode voltage equals the reference voltage applied, the output will be as shown.

Negative Series Clipper with negative V_r

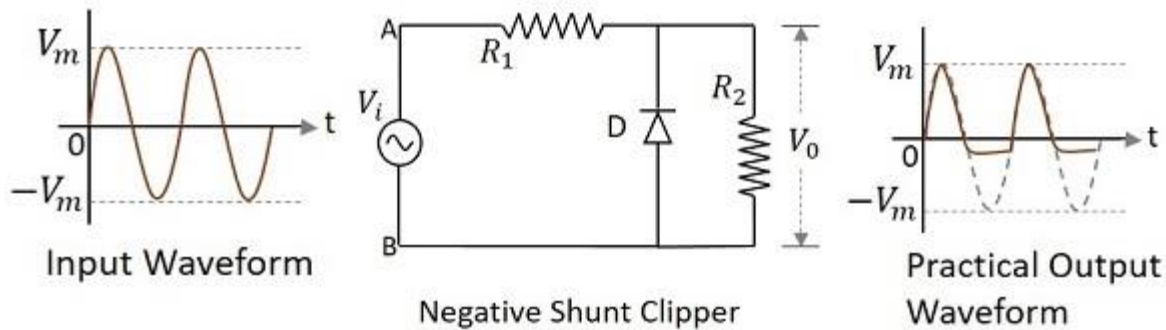
A Clipper circuit in which the diode is connected in series to the input signal and biased with negative reference voltage V_r and that attenuates the negative portions of the waveform, is termed as **Negative Series Clipper with negative V_r** . The following figure represents the circuit diagram for negative series clipper, when the reference voltage applied is negative.



During the positive cycle of the input the diode gets forward biased and the input signal appears at the output. During its negative cycle, the diode gets reverse biased and hence will not conduct. But the negative reference voltage being applied, appears at the output. Hence the negative cycle of the output waveform gets clipped after this reference level.

Negative Shunt Clipper

A Clipper circuit in which the diode is connected in shunt to the input signal and that attenuates the negative portions of the waveform, is termed as Negative Shunt Clipper. The following figure represents the circuit diagram for **negative shunt clipper**.

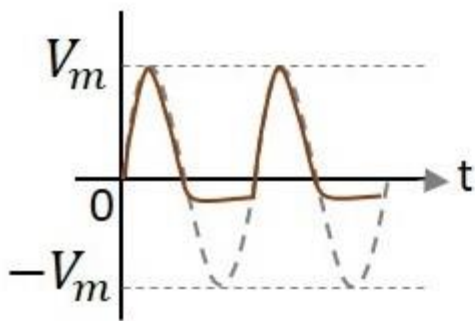


Positive Cycle of the Input – When the input voltage is applied, the positive cycle of the input makes the point A in the circuit positive with respect to the point B. This makes the diode reverse biased and hence it behaves like an open switch. Thus the voltage across the load resistor equals the applied input voltage as it completely appears at the output V_0

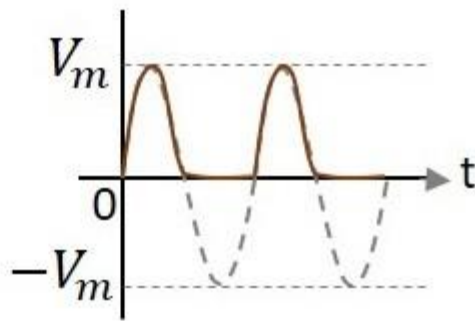
Negative Cycle of the Input – The negative cycle of the input makes the point A in the circuit negative with respect to the point B. This makes the diode forward biased and hence it conducts like a closed switch. Thus the voltage across the load resistor becomes zero as no current flows through it.

Waveforms

In the above figures, if the waveforms are observed, we can understand that just a portion of the negative peak was clipped. This is because of the voltage across V_0 . But the ideal output was not meant to be so. Let us have a look at the following figures.



Practical Output Waveform

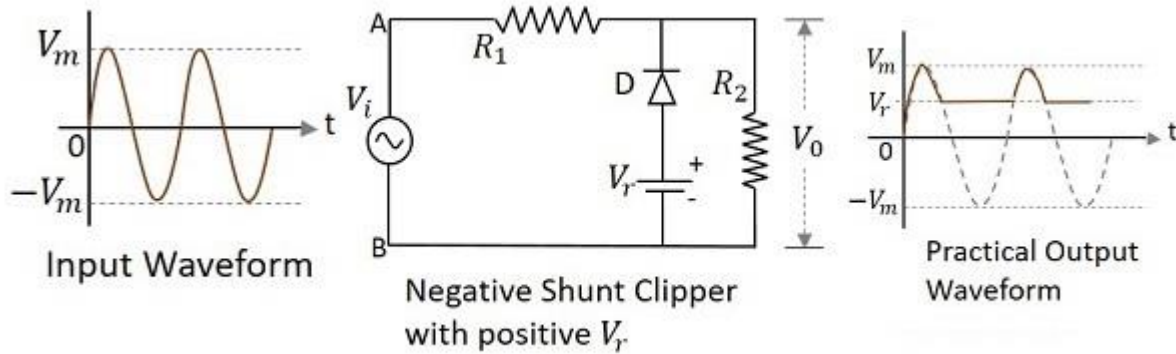


Ideal Output Waveform

Unlike the ideal output, a bit portion of the negative cycle is present in the practical output due to the diode conduction voltage which is 0.7v. Hence there will be a difference in the practical and ideal output waveforms.

Negative Shunt Clipper with positive V_r

A Clipper circuit in which the diode is connected in shunt to the input signal and biased with positive reference voltage V_r and that attenuates the negative portions of the waveform, is termed as **Negative Shunt Clipper with positive V_r** . The following figure represents the circuit diagram for negative shunt clipper when the reference voltage applied is positive.

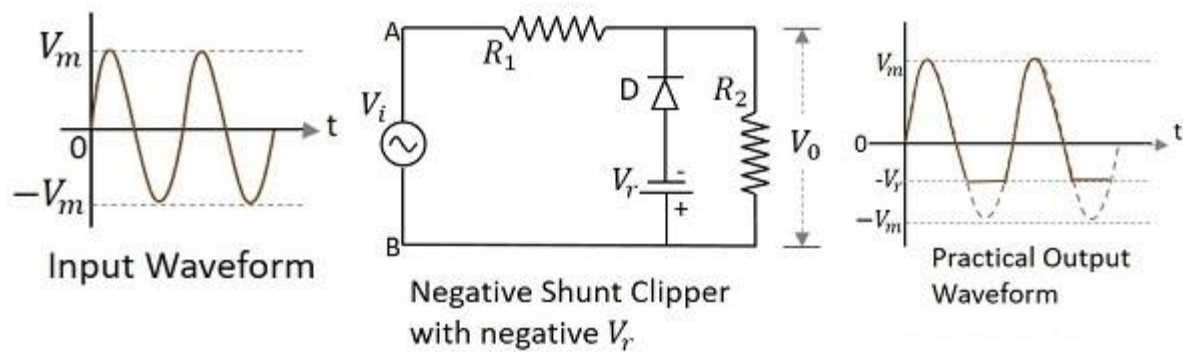


During the positive cycle of the input the diode gets reverse biased and behaves as an open switch. So whole of the input voltage, which is greater than the reference voltage applied, appears at the output. The signal below reference voltage level gets clipped off.

During the negative half cycle, as the diode gets forward biased and the loop gets completed, no output is present.

Negative Shunt Clipper with negative V_r

A Clipper circuit in which the diode is connected in shunt to the input signal and biased with negative reference voltage V_r and that attenuates the negative portions of the waveform, is termed as **Negative Shunt Clipper with negative V_r** . The following figure represents the circuit diagram for negative shunt clipper, when the reference voltage applied is negative.

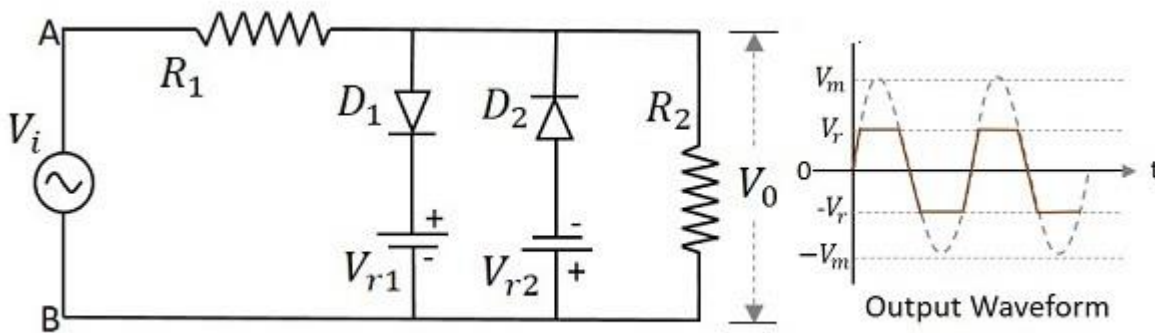


During the positive cycle of the input the diode gets reverse biased and behaves as an open switch. So whole of the input voltage, appears at the output V_o . During the negative half cycle, the diode gets forward biased. The negative voltage up to the reference voltage, gets at the output and the remaining signal gets clipped off.

Two-way Clipper

This is a positive and negative clipper with a reference voltage V_r . The input voltage is clipped two-way both positive and negative portions of the input waveform with two reference voltages. For this, two diodes D_1 and D_2 along with two reference voltages V_{r1} and V_{r2} are connected in the circuit.

This circuit is also called as a **Combinational Clipper** circuit. The figure below shows the circuit arrangement for a two-way or a combinational clipper circuit along with its output waveform.



During the positive half of the input signal, the diode D_1 conducts making the reference voltage V_{r1} appear at the output. During the negative half of the input signal, the diode D_2 conducts making the reference voltage V_{r2} appear at the output. Hence both the diodes conduct alternatively to clip the output during both the cycles. The output is taken across the load resistor.

A Clamper Circuit is a circuit that adds a DC level to an AC signal. Actually, the positive and negative peaks of the signals can be placed at desired levels using the clamping circuits. As the DC level gets shifted, a clamper circuit is called as a **Level Shifter**.

Clamper circuits consist of energy storage elements like capacitors. A simple clamper circuit comprises of a capacitor, a diode, a resistor and a dc battery if required.

Clamper Circuit

A Clamper circuit can be defined as the circuit that consists of a diode, a resistor and a capacitor that shifts the waveform to a desired DC level without changing the actual appearance of the applied signal.

In order to maintain the time period of the wave form, the τ must be greater than, half the time period. Discharging time of the capacitor should be slow. Discharging time of the capacitor should be slow.

$$\tau = RC$$

Where

- R is the resistance of the resistor employed
- C is the capacitance of the capacitor used

The time constant of charge and discharge of the capacitor determines the output of a clamper circuit.

- In a clamper circuit, a vertical shift of upward or downward takes place in the output waveform with respect to the input signal.
- The load resistor and the capacitor affect the waveform. So, the discharging time of the capacitor should be large enough.

The DC component present in the input is rejected when a capacitor coupled network is used as a capacitor blocks DC. Hence when DC needs to be restored, clamping circuit is used.

Types of Clampers

There are few types of clamper circuits, such as

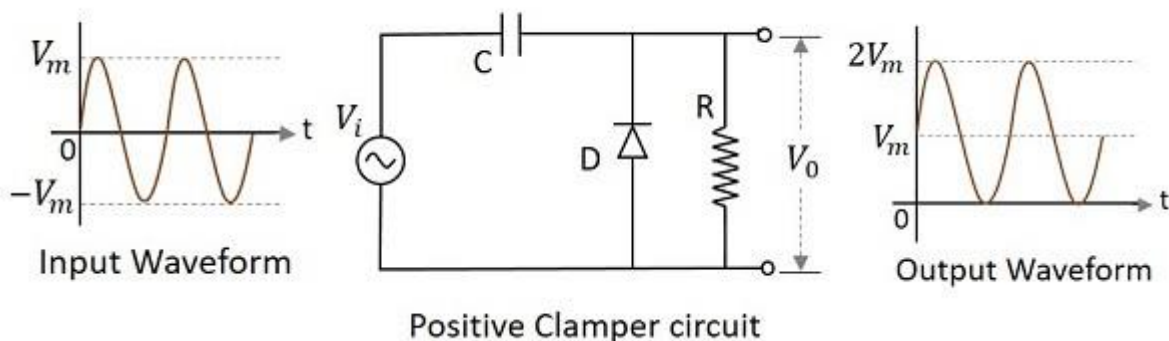
- Positive Clamper
- Positive clamper with positive V_r
- Positive clamper with negative V_r
- Negative Clamper
- Negative clamper with positive V_r
- Negative clamper with negative V_r

Let us go through them in detail.

Positive Clamper Circuit

A Clamping circuit restores the DC level. When a negative peak of the signal is raised above to the zero level, then the signal is said to be **positively clamped**.

A Positive Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the positive portion of the input signal. The figure below explains the construction of a positive clamper circuit.



Initially when the input is given, the capacitor is not yet charged and the diode is reverse biased. The output is not considered at this point of time. During the negative half cycle, at the peak value, the capacitor gets charged with negative on one plate and positive on the other. The

capacitor is now charged to its peak value V_m . The diode is forward biased and conducts heavily.

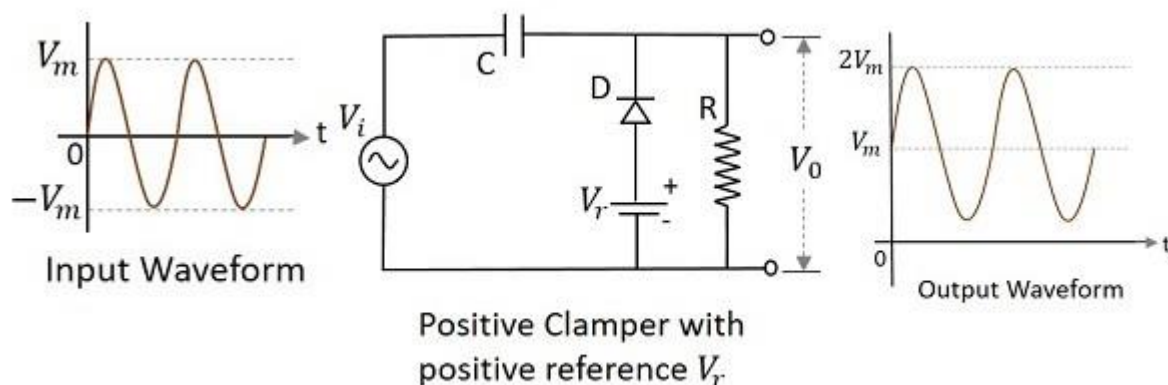
During the next positive half cycle, the capacitor is charged to positive V_m while the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be

$$V_0 = V_i + V_m$$

Hence the signal is positively clamped as shown in the above figure. The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

Positive Clamper with Positive V_r

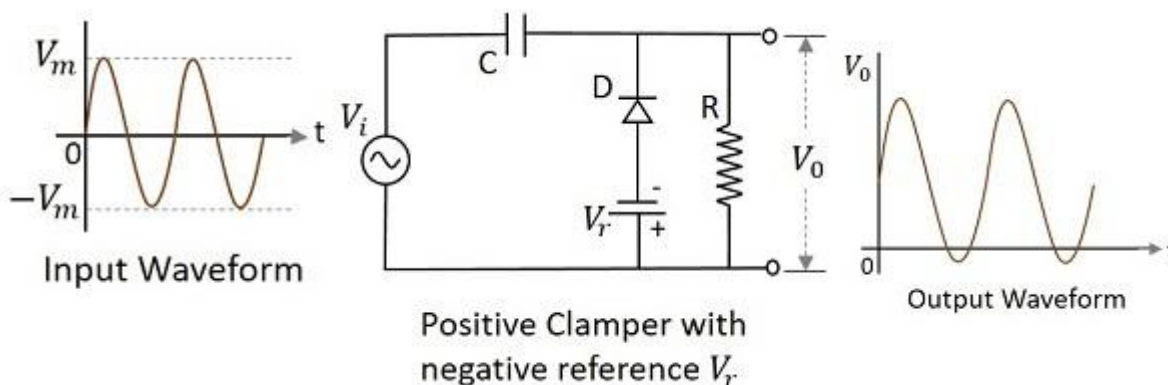
A Positive clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the positive clamper with positive reference voltage is constructed as below.



During the positive half cycle, the reference voltage is applied through the diode at the output and as the input voltage increases, the cathode voltage of the diode increase with respect to the anode voltage and hence it stops conducting. During the negative half cycle, the diode gets forward biased and starts conducting. The voltage across the capacitor and the reference voltage together maintain the output voltage level.

Positive Clamper with Negative V_r

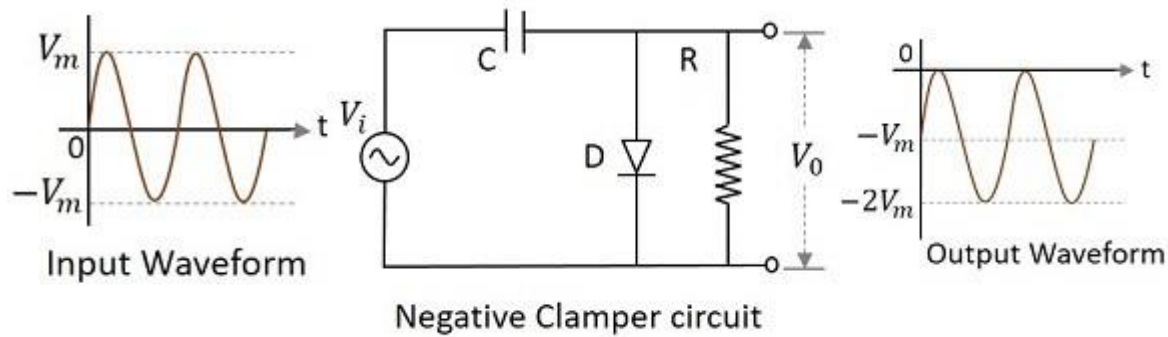
A Positive clamper circuit if biased with some negative reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the positive clamper with positive reference voltage is constructed as below.



During the positive half cycle, the voltage across the capacitor and the reference voltage together maintain the output voltage level. During the negative half-cycle, the diode conducts when the cathode voltage gets less than the anode voltage. These changes make the output voltage as shown in the above figure.

Negative Clamper

A Negative Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the negative portion of the input signal. The figure below explains the construction of a negative clamper circuit.



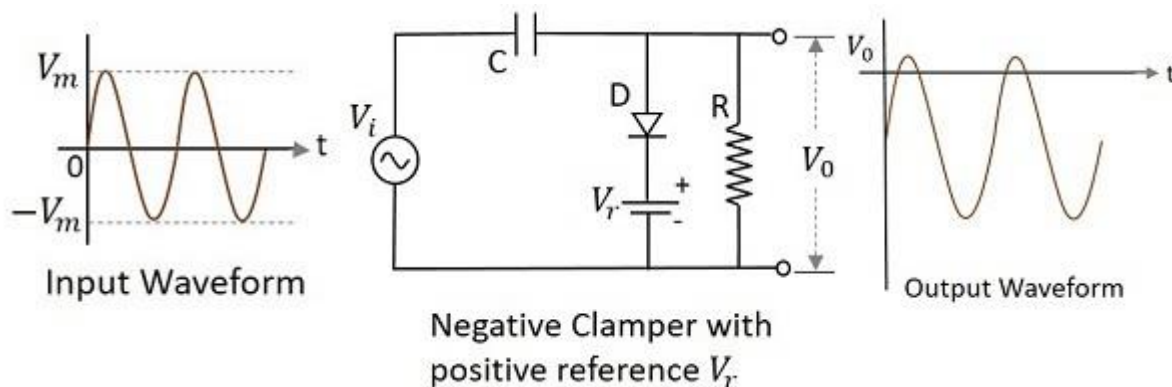
During the positive half cycle, the capacitor gets charged to its peak value v_m . The diode is forward biased and conducts. During the negative half cycle, the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be

$$V_0 = V_i + V_m$$

Hence the signal is negatively clamped as shown in the above figure. The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

Negative clamper with positive V_r

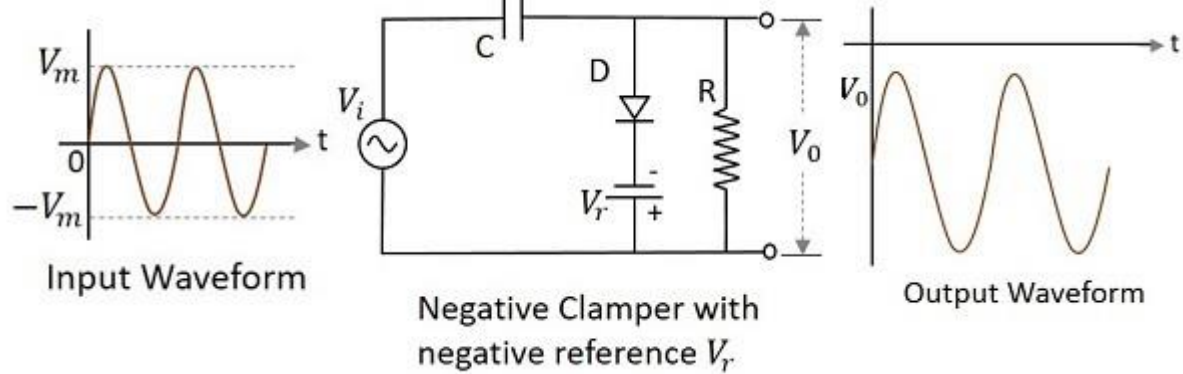
A Negative clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the negative clamper with positive reference voltage is constructed as below.



Though the output voltage is negatively clamped, a portion of the output waveform is raised to the positive level, as the applied reference voltage is positive. During the positive half-cycle, the diode conducts, but the output equals the positive reference voltage applied. During the negative half cycle, the diode acts as open circuited and the voltage across the capacitor forms the output.

Negative Clamper with Negative V_r

A Negative clamper circuit if biased with some negative reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the negative clamper with negative reference voltage is constructed as below.



The cathode of the diode is connected with a negative reference voltage, which is less than that of zero and the anode voltage. Hence the diode starts conducting during positive half cycle, before the zero voltage level. During the negative half cycle, the voltage across the capacitor appears at the output. Thus the waveform is clamped towards the negative portion.

Applications

There are many applications for both Clippers and Clampers such as

Clippers

- Used for the generation and shaping of waveforms
- Used for the protection of circuits from spikes
- Used for amplitude restorers
- Used as voltage limiters
- Used in television circuits
- Used in FM transmitters

Clampers

- Used as direct current restorers
- Used to remove distortions
- Used as voltage multipliers
- Used for the protection of amplifiers
- Used as test equipment
- Used as base-line stabilizer

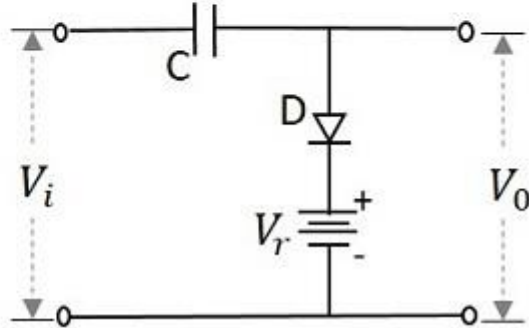
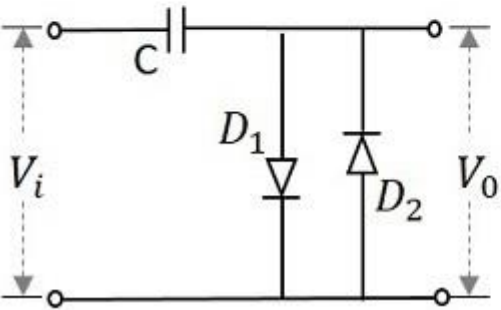
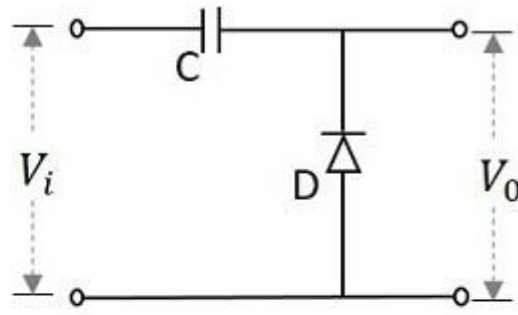
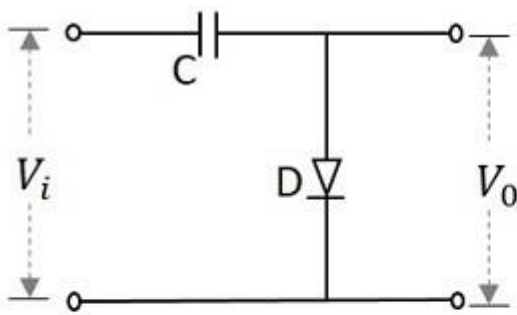
Along with the wave shaping circuits such as clippers and clampers, diodes are used to construct other circuits such as limiters and voltage multipliers, which we shall discuss in this chapter. Diodes also have another important application known as rectifiers, which will be discussed later.

Limiters

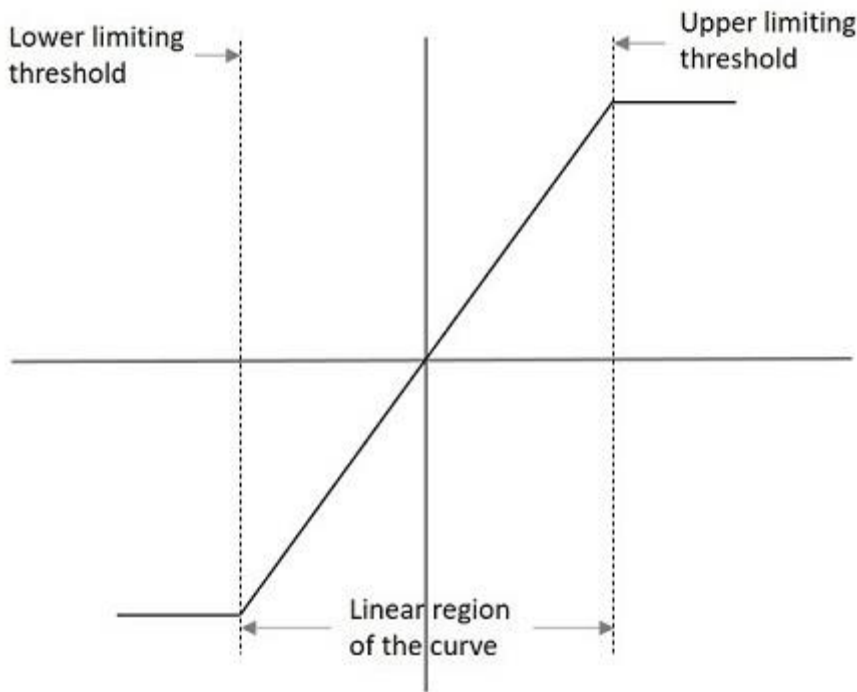
Another name which we often come across while going through these clippers and clampers is the limiter circuit. A **limiter** circuit can be understood as the one which limits the output voltage from exceeding a pre-determined value.

This is more or less a clipper circuit which does not allow the specified value of the signal to exceed. Actually clipping can be termed as an extreme extent of limiting. Hence limiting can be understood as a smooth clipping.

The following image shows some examples of limiter circuits –



The performance of a limiter circuit can be understood from its transfer characteristic curve. An example for such a curve is as follows.



The lower and upper limits are specified in the graph which indicate the limiter characteristics. The output voltage for such a graph can be understood as

$$V_0 = L_-, K V_i, L_+ \quad V_0 = L_-, K V_i, L_+$$

Where

$$L_- = V_i \leq L_- - k \quad L_- = V_i \leq L_- - k$$

$$K V_i = L_- - k < V_i < L_+ + k \quad K V_i = L_- - k < V_i < L_+ + k$$

$$L_+ = V_i \geq L_+ + K \quad L_+ = V_i \geq L_+ + K$$

Types of Limiters

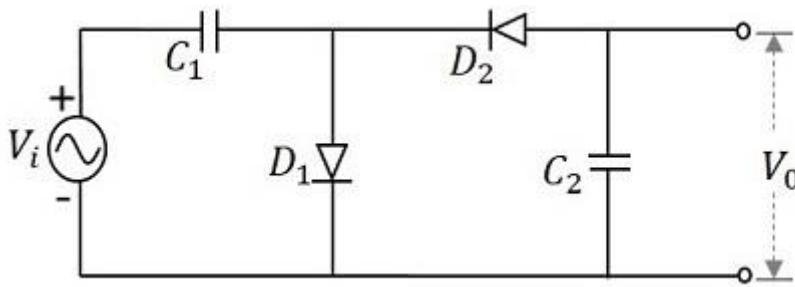
There are few types of limiters such as

- **Unipolar Limiter** – This circuit limits the signal in one way.
- **Bipolar Limiter** – This circuit limits the signal in two way.
- **Soft Limiter** – The output may change in this circuit for even a slight change in the input.
- **Hard Limiter** – The output will not easily change with the change in input signal.
- **Single Limiter** – This circuit employs one diode for limiting.
- **Double Limiter** – This circuit employs two diodes for limiting.

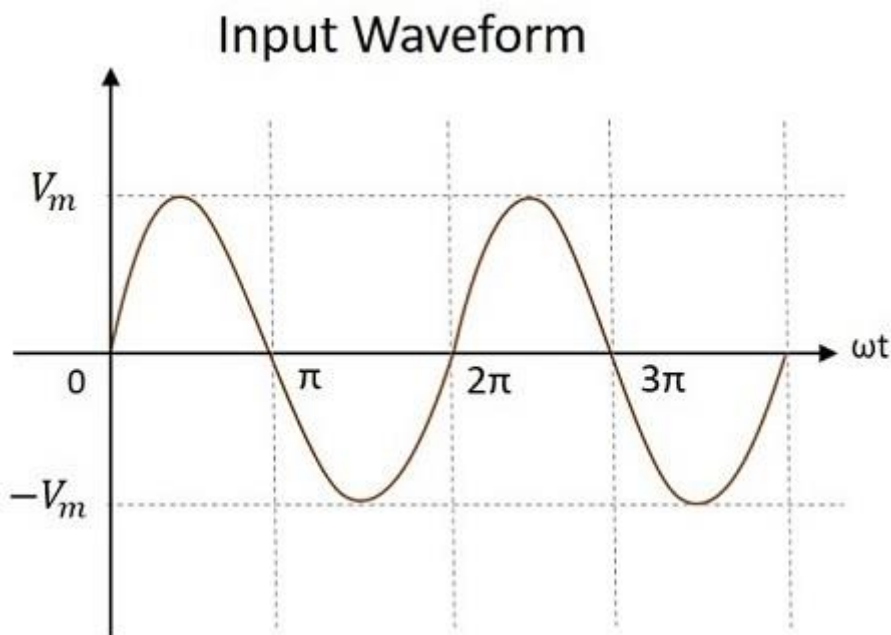
Voltage Multipliers

There are applications where the voltage needs to be multiplied in some cases. This can be done easily with the help of a simple circuit using diodes and capacitors. The voltage if doubled, such a circuit is called as a Voltage Doubler. This can be extended to make a Voltage Tripler or a Voltage Quadrupler or so on to obtain high DC voltages.

To get a better understanding, let us consider a circuit that multiplies the voltage by a factor of 2. This circuit can be called as a **Voltage Doubler**. The following figure shows the circuit of a voltage doubler.



The input voltage applied will be an AC signal which is in the form of a sine wave as shown in the figure below.

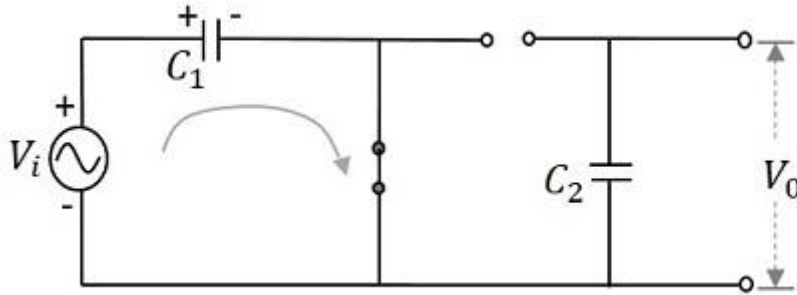


Working

The voltage multiplier circuit can be understood by analyzing each half cycle of the input signal. Each cycle makes the diodes and the capacitors work in different fashion. Let us try to understand this.

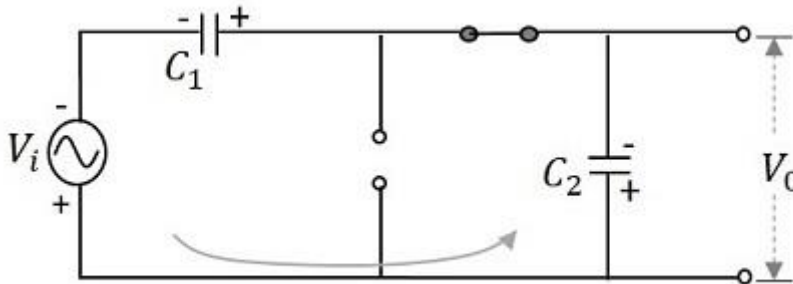
During the first positive half cycle – When the input signal is applied, the capacitor C_1 is charged and the diode D_1 is forward biased. While the diode D_2 is reverse biased and the capacitor C_2 doesn't get any charge. This makes the output V_0 to be V_m

This can be understood from the following figure.



Hence, during 0 to π , the output voltage produced will be V_{max} . The capacitor C_1 gets charged through the forward biased diode D_1 to give the output, while C_2 doesn't charge. This voltage appears at the output.

During the negative half cycle – After that, when the negative half cycle arrives, the diode D_1 gets reverse biased and the diode D_2 gets forward biased. The diode D_2 gets the charge through the capacitor C_2 which gets charged during this process. The current then flows through the capacitor C_1 which discharges. It can be understood from the following figure.



Hence during π to 2π , the voltage across the capacitor C_2 will be V_{max} . While the capacitor C_1 which is fully charged, tends to discharge. Now the voltages from both the capacitors together appear at the output, which is $2V_{max}$. So, the output voltage V_0 during this cycle is $2V_{max}$

During the next positive half cycle – The capacitor C_1 gets charged from the supply and the diode D_1 gets forward biased. The capacitor C_2 holds the charge as it will not find a way to discharge and the diode D_2 gets reverse biased. Now, the output voltage V_0 of this cycle gets the voltages from both the capacitors that together appear at the output, which is $2V_{max}$.

During the next negative half cycle – The next negative half cycle makes the capacitor C_1 to again discharge from its full charge and the diode D_1 to reverse bias while D_2 forward and capacitor C_2 to charge further to maintain its voltage. Now, the output voltage V_0 of this cycle gets the voltages from both the capacitors that together appear at the output, which is $2V_{max}$.

Hence, the output voltage V_0 is maintained to be $2V_{max}$ throughout its operation, which makes the circuit a voltage doubler.

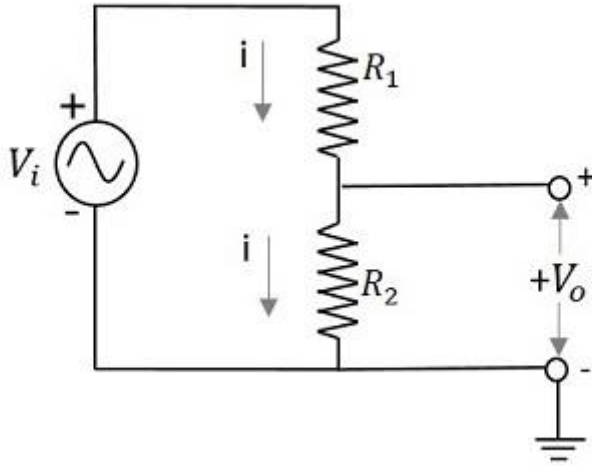
Voltage multipliers are mostly used where high DC voltages are required. For example, cathode ray tubes and computer display.

Voltage Divider

While diodes are used to multiply the voltage, a set of series resistors can be made into a small network to divide the voltage. Such networks are called as **Voltage Divider** networks.

Voltage divider is a circuit which turns a larger voltage into a smaller one. This is done using resistors connected in series. The output will be a fraction of the input. The output voltage depends upon the resistance of the load it drives.

Let us try to know how a voltage divider circuit works. The figure below is an example of a simple voltage divider network.



If we try to draw an expression for output voltage,

$$V_i = i(R_1 + R_2) \quad V_i = i(R_1 + R_2)$$

$$i = \frac{V_i}{R_1 + R_2} \quad i = \frac{V_i}{R_1 + R_2}$$

$$V_o = iR_2 \rightarrow i = \frac{V_o}{R_2} \quad V_o = iR_2 \rightarrow i = \frac{V_o}{R_2}$$

Comparing both,

$$\frac{V_o}{R_2} = \frac{V_i}{R_1 + R_2} \quad \frac{V_o}{R_2} = \frac{V_i}{R_1 + R_2}$$

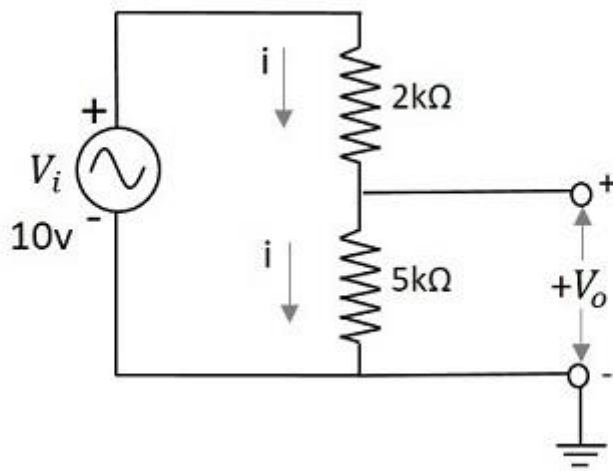
$$V_o = \frac{V_i(R_1 + R_2)}{R_2} \quad V_o = \frac{V_i(R_1 + R_2)}{R_2}$$

This is the expression to obtain the value of output voltage. Hence the output voltage is divided depending upon the resistance values of the resistors in the network. More resistors are added to have different fractions of different output voltages.

Let us have an example problem to understand more about voltage dividers.

Example

Calculate the output voltage of a network having an input voltage of 10v with two series resistors $2k\Omega$ and $5k\Omega$.



The output voltage V_0 is given by

$$\begin{aligned}
 V_0 &= V_i \frac{R_2}{R_1 + R_2} \\
 &= 10 \frac{5 \text{ k}\Omega}{2 \text{ k}\Omega + 5 \text{ k}\Omega} \\
 &= 10 \times \frac{5}{7} = 7.142 \text{ v}
 \end{aligned}$$

The output voltage V_0 for the above problem is 7.14v

Diode Switching Times

While changing the bias conditions, the diode undergoes a **transient response**. The response of a system to any sudden change from an equilibrium position is called as transient response.

The sudden change from forward to reverse and from reverse to forward bias, affects the circuit. The time taken to respond to such sudden changes is the important criterion to define the effectiveness of an electrical switch.

- The time taken before the diode recovers its steady state is called as **Recovery Time**.
- The time interval taken by the diode to switch from reverse biased state to forward biased state is called as **Forward Recovery Time**.
- The time interval taken by the diode to switch from forward biased state to reverse biased state is called as **Reverse Recovery Time**.

To understand this more clearly, let us try to analyze what happens once the voltage is applied to a switching PN diode.

Carrier Concentration

Minority charge carrier concentration reduces exponentially as seen away from the junction. When the voltage is applied, due to the forward biased condition, the majority carriers of one side move towards the other. They become minority carriers of the other side. This concentration will be more at the junction.

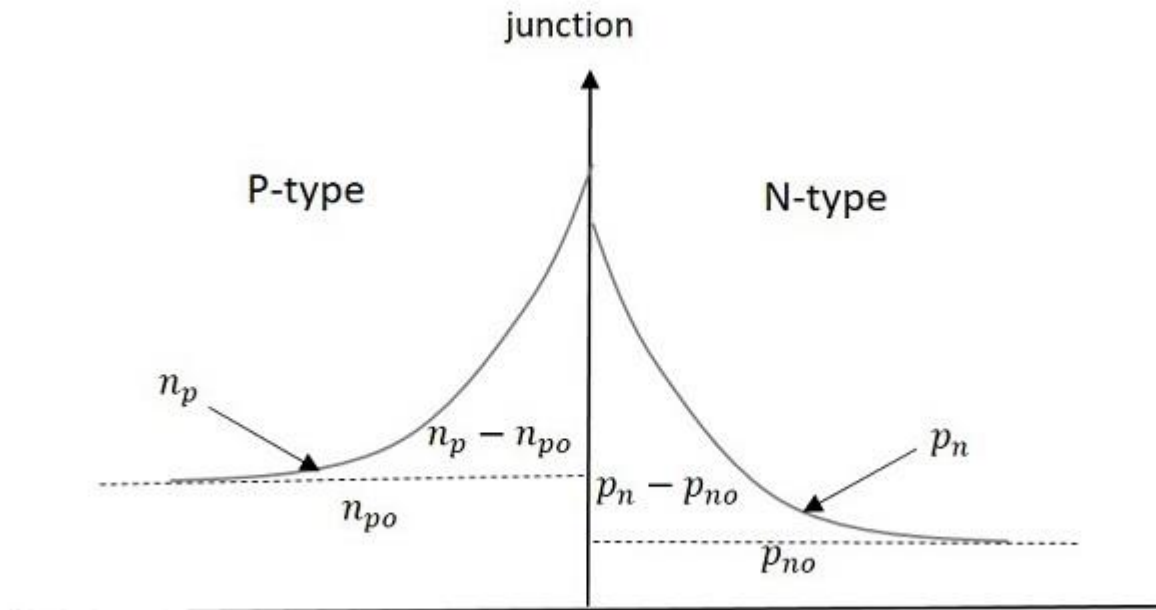
For example, if N-type is considered, the excess of holes that enter into N-type after applying forward bias, adds to the already present minority carriers of N-type material.

Let us consider few notations.

- The majority carriers in P-type holes = P_p
- The majority carriers in N-type electrons = N_n
- The minority carriers in P-type electrons = N_{p0}

- The majority carriers in N-type holesholes = PnoPno

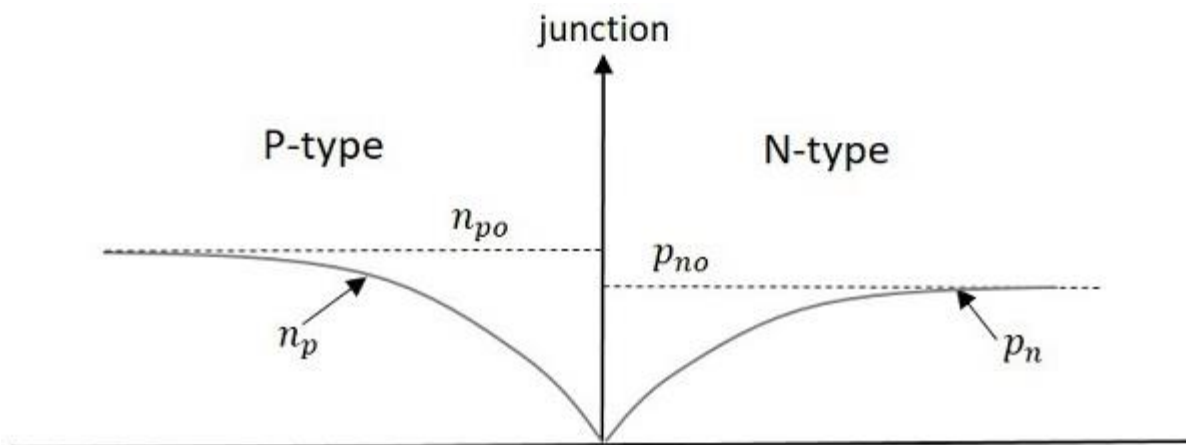
During Forward biased Condition – The minority carriers are more near junction and less far away from the junction. The graph below explains this.



Excess minority carrier charge in P-type = $n_p - n_{po}$ with n_{po} steady state value
 Excess minority carrier charge in N-type = $p_n - p_{no}$ with p_{no} steady state value

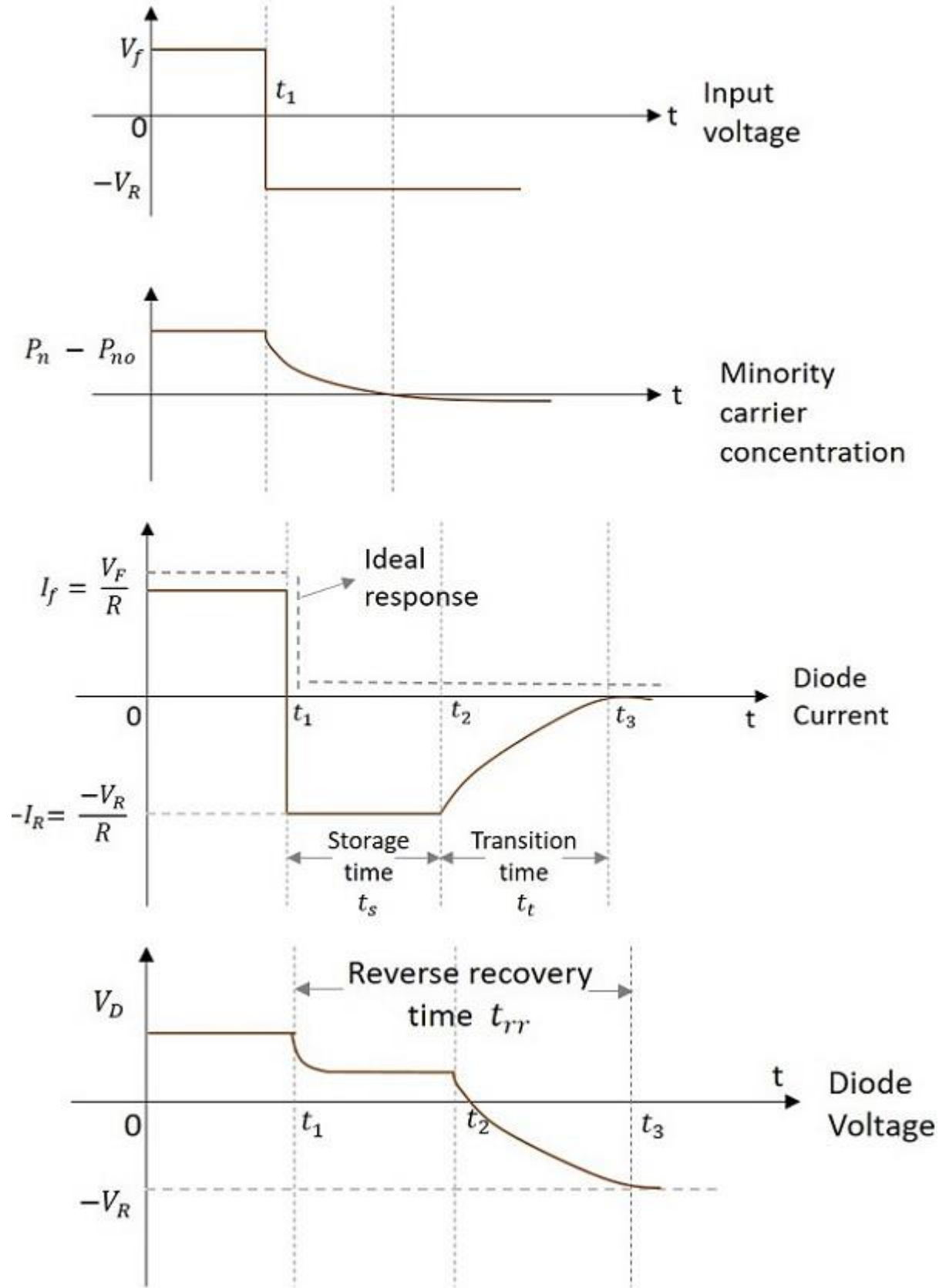
During reverse bias condition – Majority carriers doesn't conduct the current through the junction and hence don't participate in current condition. The switching diode behaves as a short circuited for an instance in reverse direction.

The minority carriers will cross the junction and conduct the current, which is called as **Reverse Saturation Current**. The following graph represents the condition during reverse bias.



In the above figure, the dotted line represents equilibrium values and solid lines represent actual values. As the current due to minority charge carriers is large enough to conduct, the circuit will be ON until this excess charge is removed.

The time required for the diode to change from forward bias to reverse bias is called **Reverse recovery time** t_{rr} . The following graphs explain the diode switching times in detail.



From the above figure, let us consider the diode current graph.

At t_1 the diode is suddenly brought to OFF state from ON state; it is known as Storage time. **Storage time** is the time required to remove the excess minority carrier charge. The negative current flowing from N to P type material is of a considerable amount during the Storage time. This negative current is,

$$-I_R = -\frac{V_R}{R}$$

The next time period is the **transition time** from t_2 to t_3

Transition time is the time taken for the diode to get completely to open circuit condition. After t_3 diode will be in steady state reverse bias condition. Before t_1 diode is under steady state forward bias condition.

So, the time taken to get completely to open circuit condition is

$$\text{Reverse recovery time}(t_{rr}) = \text{Storage time}(T_s) + \text{Transition time}(T_t)$$

Whereas to get to ON condition from OFF, it takes less time called as **Forward recovery time**. Reverse recovery time is greater than Forward recovery time. A diode works as a better switch if this Reverse recovery time is made less.

Definitions

Let us just go through the definitions of the time periods discussed.

- **Storage time** – The time period for which the diode remains in the conduction state even in the reverse biased state, is called as **Storage time**.
- **Transition time** – The time elapsed in returning back to the state of non-conduction, i.e. steady state reverse bias, is called **Transition time**.
- **Reverse recovery time** – The time required for the diode to change from forward bias to reverse bias is called as **Reverse recovery time**.
- **Forward recovery time** – The time required for the diode to change from reverse bias to forward bias is called as **Forward recovery time**.

Factors that affect diode switching times

There are few factors that affect the diode switching times, such as

- **Diode Capacitance** – The PN junction capacitance changes depending upon the bias conditions.
- **Diode Resistance** – The resistance offered by the diode to change its state.
- **Doping Concentration** – The level of doping of the diode, affects the diode switching times.
- **Depletion Width** – The narrower the width of the depletion layer, the faster the switching will be. A Zener diode has narrow depletion region than an avalanche diode, which makes the former a better switch.

Applications

There are many applications in which diode switching circuits are used, such as –

- High speed rectifying circuits
- High speed switching circuits
- RF receivers
- General purpose applications
- Consumer applications
- Automotive applications
- Telecom applications etc.

MODULE V: MULTIVIBRATORS

A **multivibrator** circuit is nothing but a **switching circuit**. It generates non-sinusoidal waves such as Square waves, Rectangular waves and Saw tooth waves etc. Multivibrators are used as frequency generators, frequency dividers and generators of time delays and also as memory elements in computers etc.

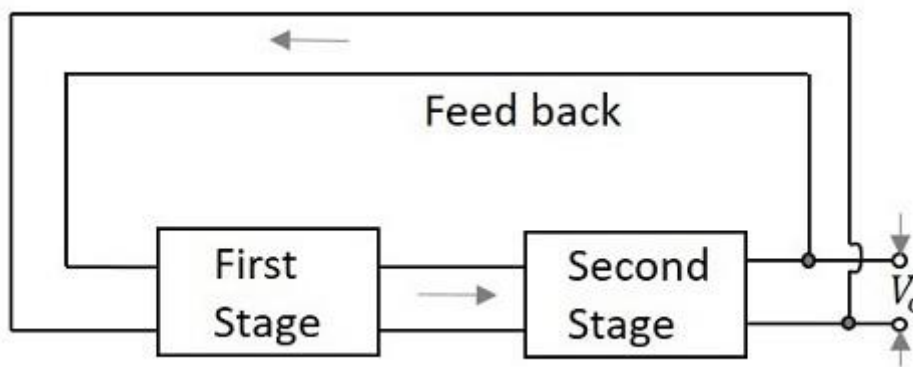
A Transistor basically functions as an amplifier in its linear region. If a transistor amplifier output stage is joined with the previous amplifier stage, such a connection is said to be coupled. If a resistor is used in coupling two stages of such an amplifier circuit, it is called as **Resistance coupled amplifier**. For more details, refer to the AMPLIFIERS tutorial.

What is a Multivibrator?

According to the definition, *A Multivibrator is a two-stage resistance coupled amplifier with positive feedback from the output of one amplifier to the input of the other.*

Two transistors are connected in feedback so that one controls the state of the other. Hence the ON and OFF states of the whole circuit, and the time periods for which the transistors are driven into saturation or cut off are controlled by the conditions of the circuit.

The following figure shows the block diagram of a Multivibrator.



Types of Multivibrators

There are two possible states of a Multivibrator. In first stage, the transistor Q_1 turns ON while the transistor Q_2 turns OFF. In second stage, the transistor Q_1 turns OFF while the transistor Q_2 turns ON. These two states are interchanged for certain time periods depending upon the circuit conditions.

Depending upon the manner in which these two states are interchanged, the Multivibrators are classified into three types. They are

Astable Multivibrator

An Astable Multivibrator is such a circuit that it **automatically switches** between the two states continuously without the application of any external pulse for its operation. As this produces a continuous square wave output, it is called as a **Free-running Multivibrator**. The dc power source is a common requirement.

The time period of these states depends upon the time constants of the components used. As the Multivibrator keeps on switching, these states are known as quasi-stable or halfstable states. Hence there are **two quasi-stable states** for an Astable Multivibrator.

Monostable Multivibrator

A Monostable Multivibrator has a **stable state** and a **quasi-stable state**. This has a trigger input to one transistor. So, one transistor changes its state automatically, while the other one needs a trigger input to change its state.

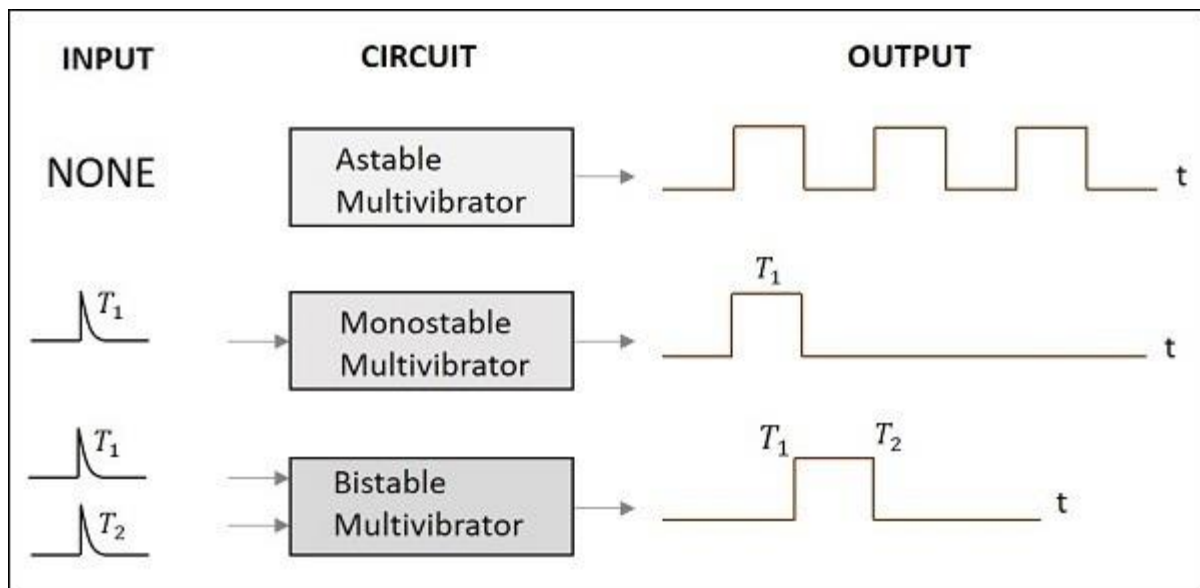
As this Multivibrator produces a single output for each trigger pulse, this is known as **One-shot Multivibrator**. This Multivibrator cannot stay in quasi-stable state for a longer period while it stays in stable state until the trigger pulse is received.

Bistable Multivibrator

A Bistable Multivibrator has both the **two states stable**. It requires two trigger pulses to be applied to change the states. Until the trigger input is given, this Multivibrator cannot change its state. It's also known as **flip-flop multivibrator**.

As the trigger pulse sets or resets the output, and as some data, i.e., either high or low is stored until it is disturbed, this Multivibrator can be called as a **Flip-flop**. To know more about flip-flops, refer our **DIGITAL CIRCUITS** tutorial at: https://www.tutorialspoint.com/digital_circuits/index.htm

To get a clear idea on the above discussion, let us have a look at the following figure.

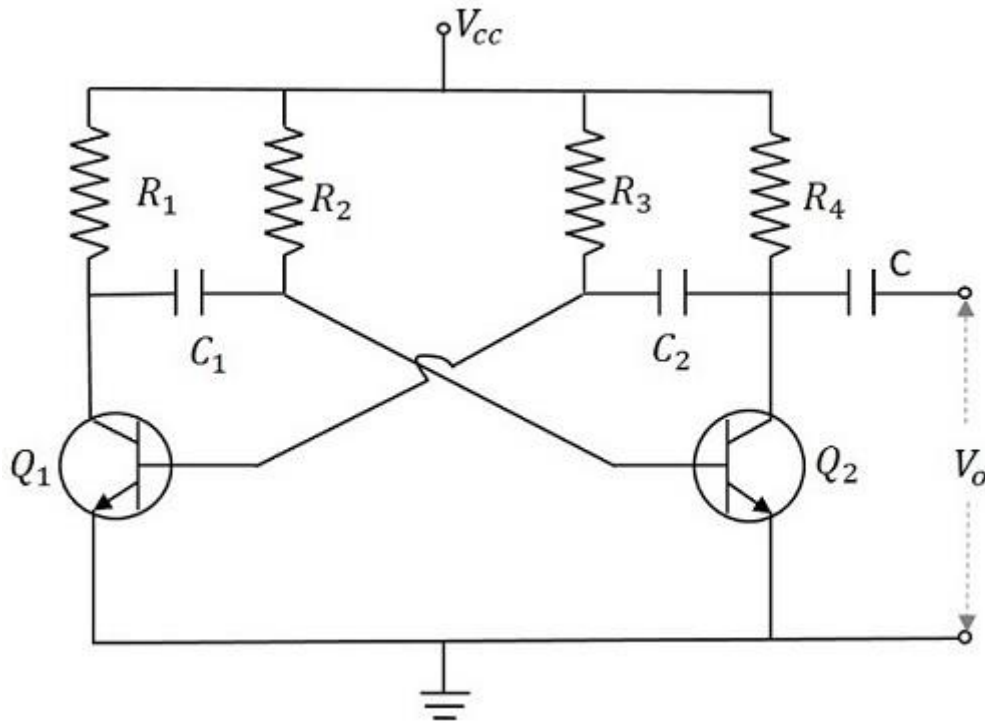


An astable multivibrator has **no stable states**. Once the Multivibrator is ON, it just changes its states on its own after a certain time period which is determined by the R_C time constants. A dc power supply or V_{cc} is given to the circuit for its operation.

Construction of Astable Multivibrator

Two transistors named Q_1 and Q_2 are connected in feedback to one another. The collector of transistor Q_1 is connected to the base of transistor Q_2 through the capacitor C_1 and vice versa. The emitters of both the transistors are connected to the ground. The collector load resistors R_1 and R_4 and the biasing resistors R_2 and R_3 are of equal values. The capacitors C_1 and C_2 are of equal values.

The following figure shows the circuit diagram for Astable Multivibrator.



Operation of Astable Multivibrator

When V_{cc} is applied, the collector current of the transistors increase. As the collector current depends upon the base current,

$$I_c = \beta I_B \quad I_c = \beta I_B$$

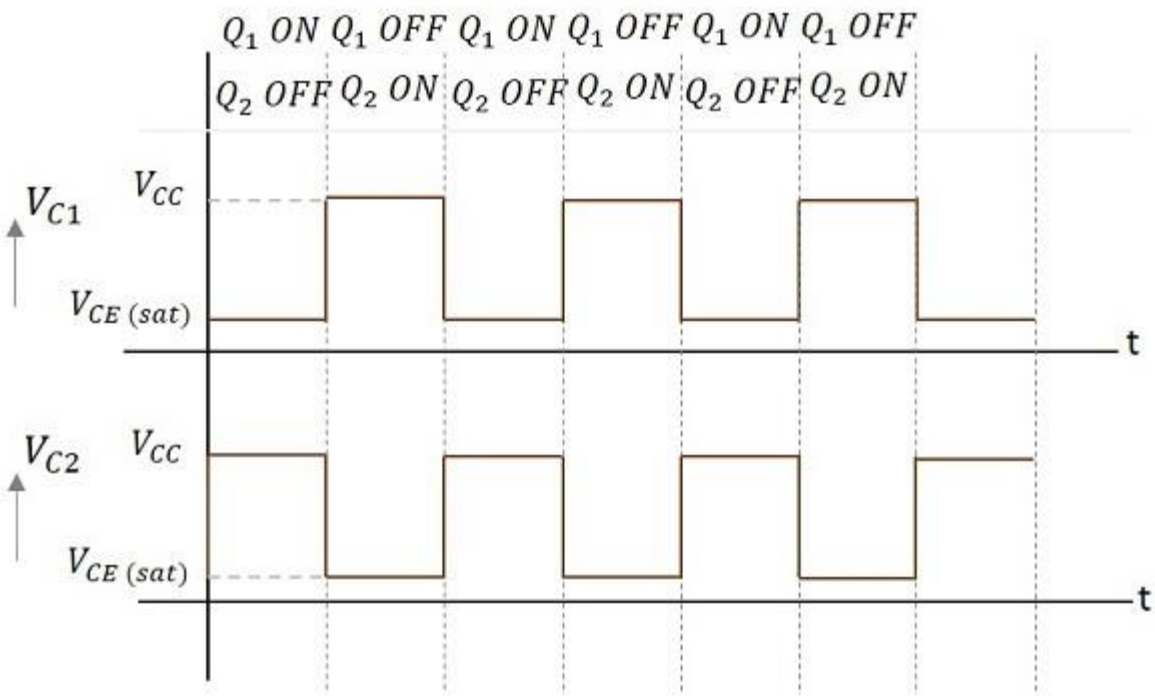
As no transistor characteristics are alike, one of the two transistors say Q_1 has its collector current increase and thus conducts. The collector of Q_1 is applied to the base of Q_2 through C_1 . This connection lets the increased negative voltage at the collector of Q_1 to get applied at the base of Q_2 and its collector current decreases. This continuous action makes the collector current of Q_2 to decrease further. This current when applied to the base of Q_1 makes it more negative and with the cumulative actions Q_1 gets into saturation and Q_2 to cut off. Thus the output voltage of Q_1 will be $V_{CE(sat)}$ and Q_2 will be equal to V_{CC} .

The capacitor C_1 charges through R_1 and when the voltage across C_1 reaches $0.7v$, this is enough to turn the transistor Q_2 to saturation. As this voltage is applied to the base of Q_2 , it gets into saturation, decreasing its collector current. This reduction of voltage at point B is applied to the base of transistor Q_1 through C_2 which makes the Q_1 reverse bias. A series of these actions turn the transistor Q_1 to cut off and transistor Q_2 to saturation. Now point A has the potential V_{CC} . The capacitor C_2 charges through R_2 . The voltage across this capacitor C_2 when gets to $0.7v$, turns on the transistor Q_1 to saturation.

Hence the output voltage and the output waveform are formed by the alternate switching of the transistors Q_1 and Q_2 . The time period of these ON/OFF states depends upon the values of biasing resistors and capacitors used, i.e., on the R_C values used. As both the transistors are operated alternately, the output is a square waveform, with the peak amplitude of V_{CC} .

Waveforms

The output waveforms at the collectors of Q_1 and Q_2 are shown in the following figures.



Frequency of Oscillations

The ON time of transistor Q_1 or the OFF time of transistor Q_2 is given by

$$t_1 = 0.69R_1C_1$$

Similarly, the OFF time of transistor Q_1 or ON time of transistor Q_2 is given by

$$t_2 = 0.69R_2C_2$$

Hence, total time period of square wave

$$t = t_1 + t_2 = 0.69(R_1C_1 + R_2C_2)$$

As $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency of square wave will be

$$f = \frac{1}{t} = \frac{1}{11.38RC} = 0.07RC$$

Advantages

The advantages of using an astable multivibrator are as follows –

- No external triggering required.
- Circuit design is simple
- Inexpensive
- Can function continuously

Disadvantages

The drawbacks of using an astable multivibrator are as follows –

- Energy absorption is more within the circuit.
- Output signal is of low energy.
- Duty cycle less than or equal to 50% can't be achieved.

Applications

Astable Multivibrators are used in many applications such as amateur radio equipment, Morse code generators, timer circuits, analog circuits, and TV systems.

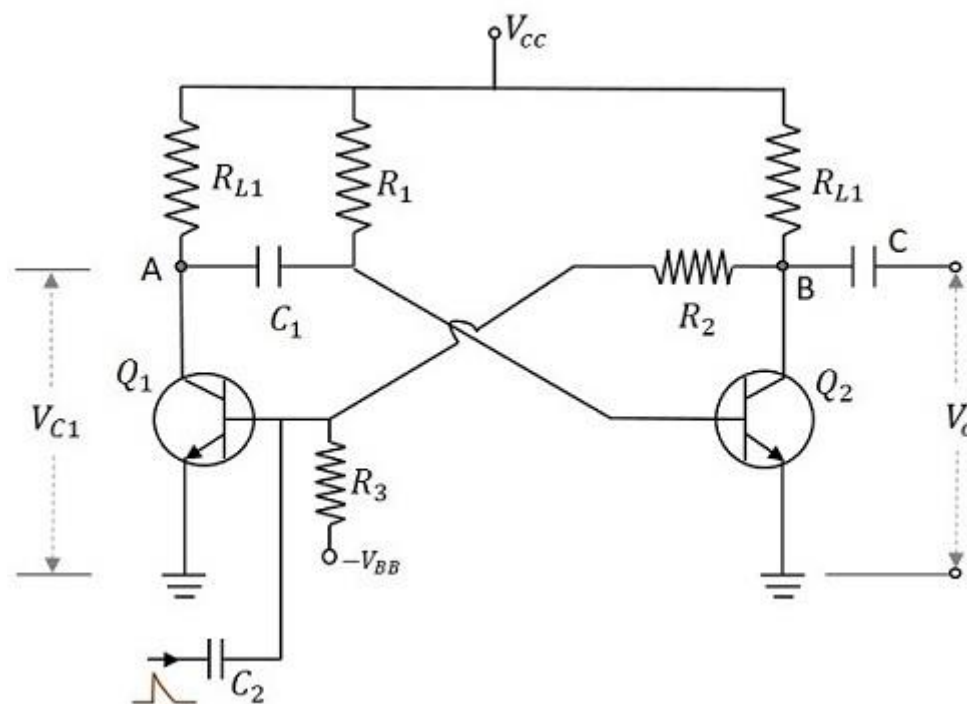
A monostable multivibrator, as the name implies, has only **one stable state**. When the transistor conducts, the other remains in non-conducting state. A stable state is such a state where the transistor remains without being altered, unless disturbed by some external trigger pulse. As Monostable works on the same principle, it has another name called as **One-shot Multivibrator**.

Construction of Monostable Multivibrator

Two transistors Q_1 and Q_2 are connected in feedback to one another. The collector of transistor Q_1 is connected to the base of transistor Q_2 through the capacitor C_1 . The base Q_1 is connected to the collector of Q_2 through the resistor R_2 and capacitor C . Another dc supply voltage $-V_{BB}$ is given to the base of transistor Q_1 through the resistor R_3 . The trigger pulse is given to the base of Q_1 through the capacitor C_2 to change its state. R_{L1} and R_{L2} are the load resistors of Q_1 and Q_2 .

One of the transistors, when gets into a stable state, an external trigger pulse is given to change its state. After changing its state, the transistor remains in this quasi-stable state or Meta-stable state for a specific time period, which is determined by the values of RC time constants and gets back to the previous stable state.

The following figure shows the circuit diagram of a Monostable Multivibrator.



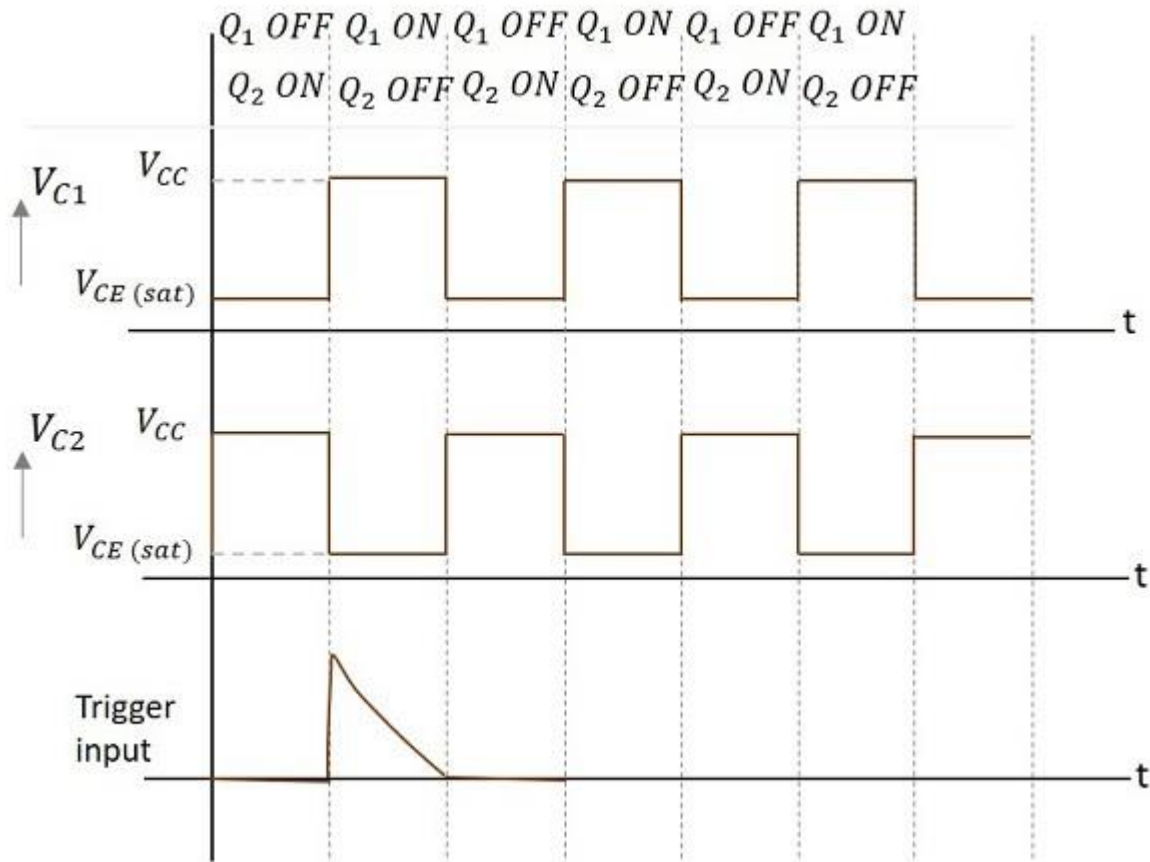
Operation of Monostable Multivibrator

Firstly, when the circuit is switched ON, transistor Q_1 will be in OFF state and Q_2 will be in ON state. This is the stable state. As Q_1 is OFF, the collector voltage will be V_{CC} at point A and hence C_1 gets charged. A positive trigger pulse applied at the base of the transistor Q_1 turns the transistor ON. This decreases the collector voltage, which turns OFF the transistor Q_2 . The capacitor C_1 starts discharging at this point of time. As the positive voltage from the collector of transistor Q_2 gets applied to transistor Q_1 , it remains in ON state. This is the quasi-stable state or Meta-stable state.

The transistor Q_2 remains in OFF state, until the capacitor C_1 discharges completely. After this, the transistor Q_2 turns ON with the voltage applied through the capacitor discharge. This turn ON the transistor Q_1 , which is the previous stable state.

Output Waveforms

The output waveforms at the collectors of Q_1 and Q_2 along with the trigger input given at the base of Q_1 are shown in the following figures.



The width of this output pulse depends upon the RC time constant. Hence it depends on the values of R_1C_1 . The duration of pulse is given by

$$T=0.69R_1C_1$$

The trigger input given will be of very short duration, just to initiate the action. This triggers the circuit to change its state from Stable state to Quasi-stable or Meta-stable or Semi-stable state, in which the circuit remains for a short duration. There will be one output pulse for one trigger pulse.

Advantages

The advantages of Monostable Multivibrator are as follows –

- One trigger pulse is enough.
- Circuit design is simple
- Inexpensive

Disadvantages

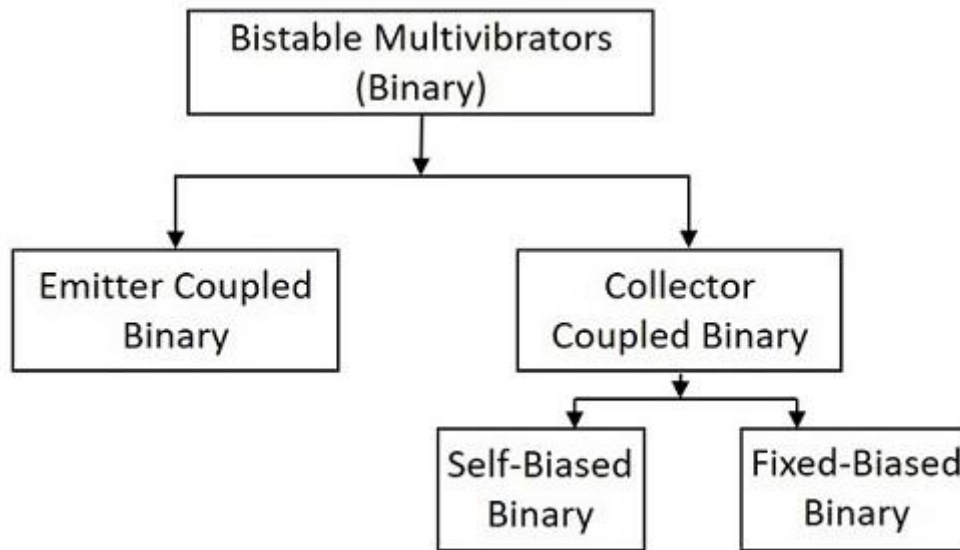
The major drawback of using a monostable multivibrator is that the time between the applications of trigger pulse T has to be greater than the RC time constant of the circuit.

Applications

Monostable Multivibrators are used in applications such as television circuits and control system circuits.

A Bistable Multivibrator has **two stable states**. The circuit stays in any one of the two stable states. It continues in that state, unless an external trigger pulse is given. This Multivibrator is also known as **Flip-flop**. This circuit is simply called as **Binary**.

There are few types in Bistable Multivibrators. They are as shown in the following figure.

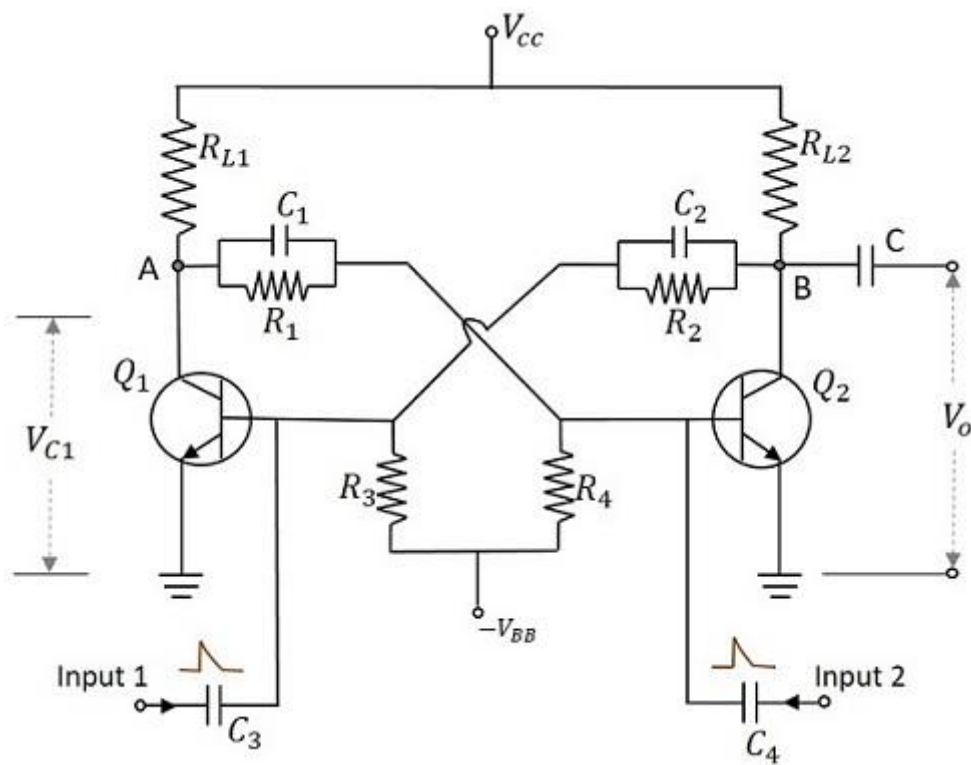


Construction of Bistable Multivibrator

Two similar transistors Q_1 and Q_2 with load resistors R_{L1} and R_{L2} are connected in feedback to one another. The base resistors R_3 and R_4 are joined to a common source $-V_{BB}$. The feedback resistors R_1 and R_2 are shunted by capacitors C_1 and C_2 known as **Commutating Capacitors**. The transistor Q_1 is given a trigger input at the base through the capacitor C_3 and the transistor Q_2 is given a trigger input at its base through the capacitor C_4 .

The capacitors C_1 and C_2 are also known as **Speed-up Capacitors**, as they reduce the **transition time**, which means the time taken for the transfer of conduction from one transistor to the other.

The following figure shows the circuit diagram of a self-biased Bistable Multivibrator.



Operation of Bistable Multivibrator

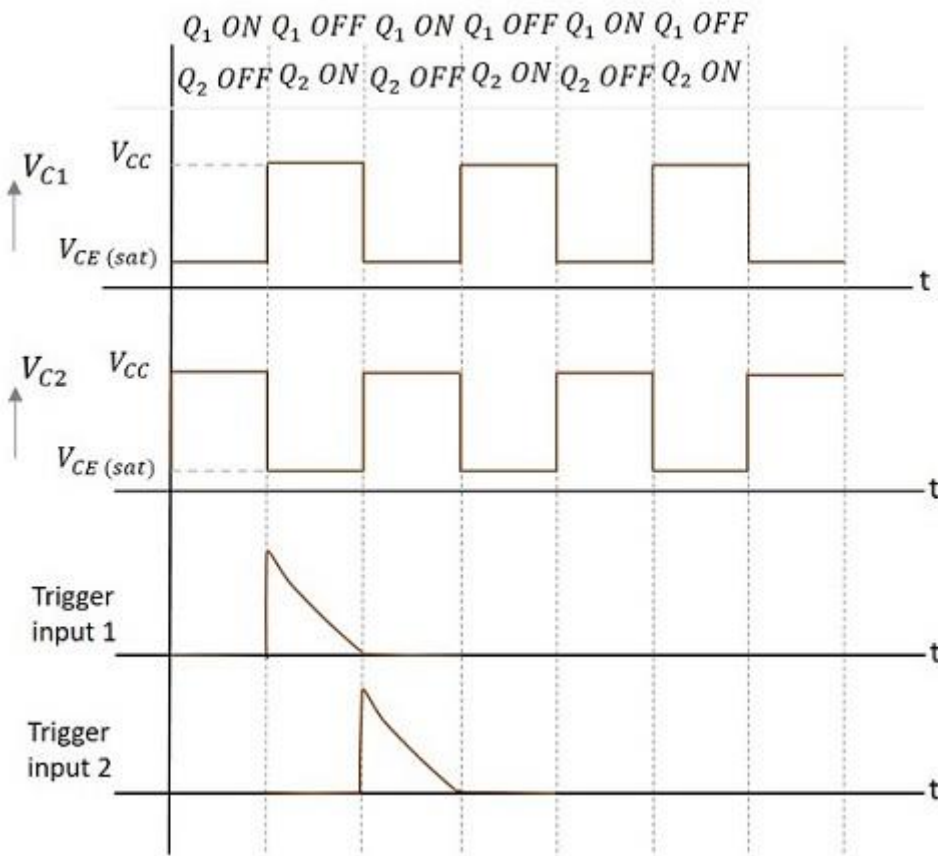
When the circuit is switched ON, due to some circuit imbalances as in Astable, one of the transistors, say Q_1 gets switched ON, while the transistor Q_2 gets switched OFF. This is a stable state of the Bistable Multivibrator.

By applying a negative trigger at the base of transistor Q_1 or by applying a positive trigger pulse at the base of transistor Q_2 , this stable state is unaltered. So, let us understand this by considering a negative pulse at the base of transistor Q_1 . As a result, the collector voltage increases, which forward biases the transistor Q_2 . The collector current of Q_2 as applied at the base of Q_1 , reverse biases Q_1 and this cumulative action, makes the transistor Q_1 OFF and transistor Q_2 ON. This is another stable state of the Multivibrator.

Now, if this stable state has to be changed again, then either a negative trigger pulse at transistor Q_2 or a positive trigger pulse at transistor Q_1 is applied.

Output Waveforms

The output waveforms at the collectors of Q_1 and Q_2 along with the trigger inputs given at the bases of Q_1 and Q_2 are shown in the following figures.



Advantages

The advantages of using a Bistable Multivibrator are as follows –

- Stores the previous output unless disturbed.
- Circuit design is simple

Disadvantages

The drawbacks of a Bistable Multivibrator are as follows –

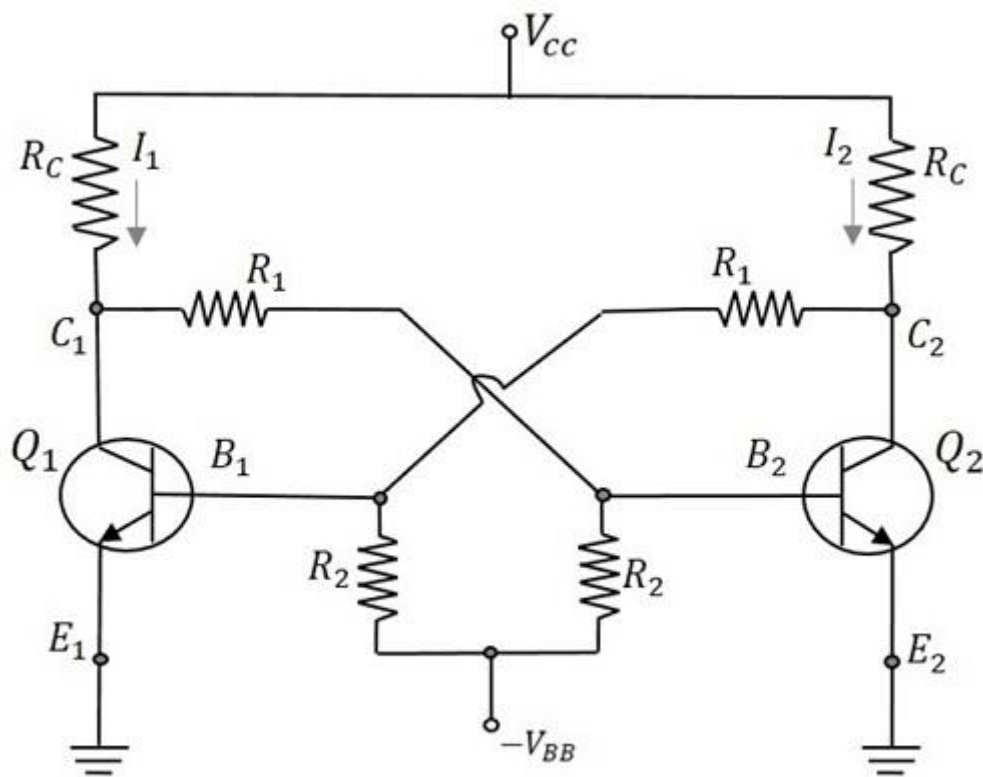
- Two kinds of trigger pulses are required.
- A bit costlier than other Multivibrators.

Applications

Bistable Multivibrators are used in applications such as pulse generation and digital operations like counting and storing of binary information.

Fixed-bias Binary

A fixed-bias binary circuit is similar to an Astable Multivibrator but with a simple SPDT switch. Two transistors are connected in feedback with two resistors, having one collector connected to the base of the other. The figure below shows the circuit diagram of a fixed-bias binary.



To understand the operation, let us consider the switch to be in position 1. Now the transistor Q_1 will be OFF as the base is grounded. The collector voltage at the output terminal V_{O1} will be equal to V_{CC} which turns the transistor Q_2 ON. The output at the terminal V_{O2} goes LOW. This is a stable state which can be altered only by an external trigger. The change of switch to position 2, works as a trigger.

When the switch is altered, the base of transistor Q_2 is grounded turning it to OFF state. The collector voltage at V_{O2} will be equal to V_{CC} which is applied to transistor Q_1 to turn it ON. This is the other stable state. The triggering is achieved in this circuit with the help of a SPDT Switch.

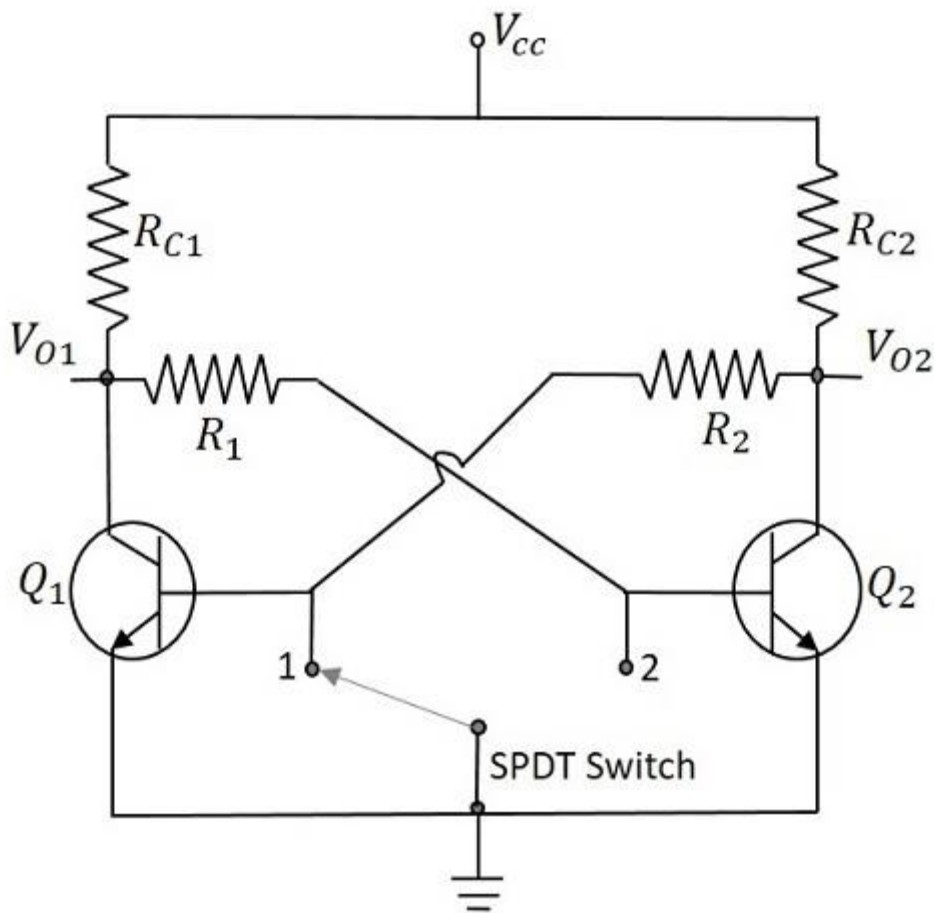
There are two main types of triggering given to the binary circuits. They are

- Symmetrical Triggering
- Asymmetrical Triggering

Schmitt Trigger

Another type of binary circuit which is ought to be discussed is the **Emitter Coupled Binary Circuit**. This circuit is also called as **Schmitt Trigger** circuit. This circuit is considered as a special type of its kind for its applications.

The main difference in the construction of this circuit is that the coupling from the output C_2 of the second transistor to the base B_1 of the first transistor is missing and that feedback is obtained now through the resistor R_e . This circuit is called as the **Regenerative circuit** for this has a **positive feedback** and **no Phase inversion**. The circuit of Schmitt trigger using BJT is as shown below.



Initially we have Q_1 OFF and Q_2 ON. The voltage applied at the base of Q_2 is V_{CC} through R_{C1} and R_1 . So the output voltage will be

$$V_0 = V_{CC} - (I_{C2} R_{C2})$$

As Q_2 is ON, there will be a voltage drop across R_E , which will be $(I_{C2} + I_{B2}) R_E$. Now this voltage gets applied at the emitter of Q_1 . The input voltage is increased and until Q_1 reaches cut-in voltage to turn ON, the output remains LOW. With Q_1 ON, the output will increase as Q_2 is also ON. As the input voltage continues to rise, the voltage at the points C_1 and B_2 continue to fall and E_2 continues to rise. At certain value of the input voltage, Q_2 turns OFF. The output voltage at this point will be V_{CC} and remains constant though the input voltage is further increased.

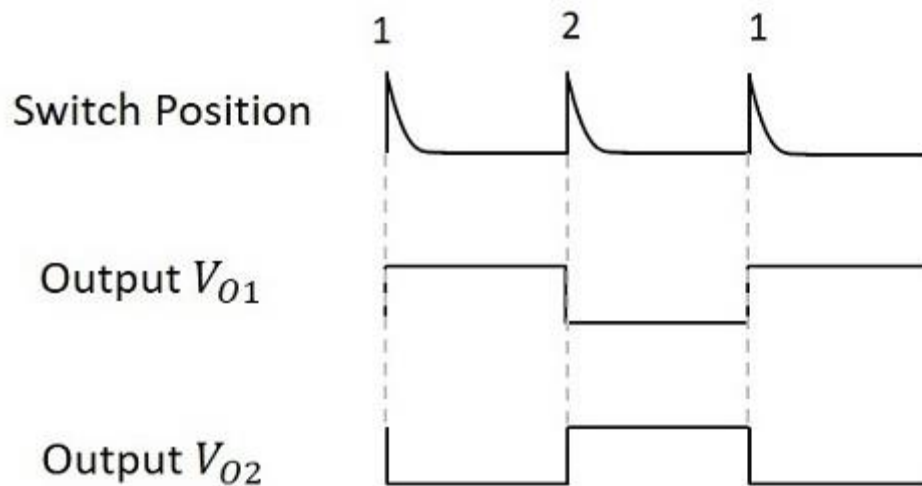
As the input voltage rises, the output remains LOW until the input voltage reaches V_1 where

$$V_1 = [V_{CC} - (I_{C2} R_{C2})]$$

The value where the input voltage equals V_1 , lets the transistor Q_1 to enter into saturation, is called **UTP** (Upper Trigger Point). If the voltage is already greater than V_1 , then it remains there until the input voltage reaches V_2 , which is a low level transition. Hence the value for which input voltage will be V_2 at which Q_2 gets into ON condition, is termed as **LTP** (Lower Trigger Point).

Output Waveforms

The output waveforms are obtained as shown below.



The Schmitt trigger circuit works as a **Comparator** and hence compares the input voltage with two different voltage levels called as **UTP** (Upper Trigger Point) and **LTP** (Lower Trigger Point). If the input crosses this UTP, it is considered as a **HIGH** and if it gets below this LTP, it is taken as a **LOW**. The output will be a binary signal indicating 1 for **HIGH** and 0 for **LOW**. Hence an analog signal is converted into a digital signal. If the input is at intermediate value (between **HIGH** and **LOW**) then the previous value will be the output.

This concept depends upon the phenomenon called as **Hysteresis**. The transfer characteristics of electronic circuits exhibit a **loop** called as **Hysteresis**. It explains that the output values depends upon both the present and the past values of the input. This prevents unwanted frequency switching in Schmitt trigger circuits

Advantages

The advantages of Schmitt trigger circuit are

- Perfect logic levels are maintained.
- It helps avoiding Meta-stability.
- Preferred over normal comparators for its pulse conditioning.

Disadvantages

The main disadvantages of a Schmitt trigger are

- If the input is slow, the output will be slower.
- If the input is noisy, the output will be noisier.

Applications of Schmitt trigger

Schmitt trigger circuits are used as Amplitude Comparator and Squaring Circuit. They are also used in Pulse conditioning and sharpening circuits.